

PAGE	TITLE
01	INDEX
02	BLOCK DIAGRAM
03	CLOCKS/SMBUS DIAGRAM
04	POWER DISTRIBUTION DIAGRAM
05	POWER SEQUENCE DIAGRAM
06	GPIO TABLE
07	AM4 PCIE GFX/HUB/SATA
08	AM4 DP/MISC
09	AM4 ACPI/AZ/SMBUS
10	AM4 CLOCK/USB/SPI/LPC
11	AM4 DDR 4 CHANNEL A
12	AM4 DDR 4 CHANNEL B
13	AM4 POWER-1
14	AM4 POWER-2
15	AM4 GND/RSVD
16	AM4 HDT+
17	Blank
18	DDR4_CHA_DIMM1-XMM2-BLACK
19	Blank
20	DDR4_CHB_DIMM1-XMM1-BLACK
21	PM - DMI/GPP/SATA/CLK
22	PM - USB
23	PM - POWER
24	PM - GPIO/ACPI/MISC
25	PM - GND/PLL
26	PM - STRAP
27	PCIE-X16
28	PCIE-X1
29	HDMI2
30	HDMI1
31	AUDIO ALC3863
32	AUDIO CONNECTOR
33	FRONT PANEL
34	SPI EEPROM&LPC DEBUG
35	M2_2280-KEYM SSD
36	M2_2230-KEYA WLAN
37	RTL8161GSH
38	RJ45/BLEED OFF/USB X2
39	SATA
40	USB POWER
41	FRONT USB
42	REAR USB
43	SIO ITE8732
44	FAN HEADER
45	LED/HEADER/BUZZER
46	POWER CONN&EMI CAP
47	MECHANICAL PART
48	AMD PWRGD CKT
49	TYPEC PD CONTROLLER
50	+3.3V_LPS
51	+3.3V_AUX
52	+5V_AUX & +5V_DUAL
53	+1.05V_AUX & +1.05V_MAIN
54	+1.8V_AUX & +1.8V_MAIN
55	+1.5V_AUX
56	+VDDP_S5 & +VDDP
57	+VPP & +2.5V_MAIN
58	+VDDIO_MEM
59	+VTT_DDR
60	+5V_TYPEC
61	+VCORE CONTROLLER
62	+VDDCR_CPU PHASE 1 & 2
63	+VDDCR_CPU PHASE 3 & 4
64	+VDDCR_SOC PHASE 1 & 2
65	+0.775V_AUX & +VDDCR_SOC_S5
66	CURRENT MONITOR & UVP
67	PWR Change list
68	Change List

AMD AM4 APU-BASED PLATFORM

APU: AM4 Bristol Ridge/Summit Ridge/ Raven Ridge
Chipset: Promontory 2


Project Information

Name: Basswood
Phase:SMVB
Ver: X4
SVID: 103C
SSID: 8399
Form factor:uATX

Project	Description	PCA PN	SCH PN (DG#)	PCB PN	ASSY CODE
Basswood	MB,Basswood,AM4,PROM2,MT	921821-001	921822-000	921823-001	GHPV

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
DB1	RED	YELLOW
DB2	RED	WHITE
SH1	LIGHT BLUE	YELLOW
SH2+	LIGHT BLUE	WHITE
PV1	GREEN	YELLOW
PV2+	GREEN	WHITE
MVB / PRODUCTION	GREEN	WHITE



HP RESTRICTED (HP RESTRICTED SECRET)
THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION
THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY
FOXCONN

File

Index

Size
C

Document Number
921822-000

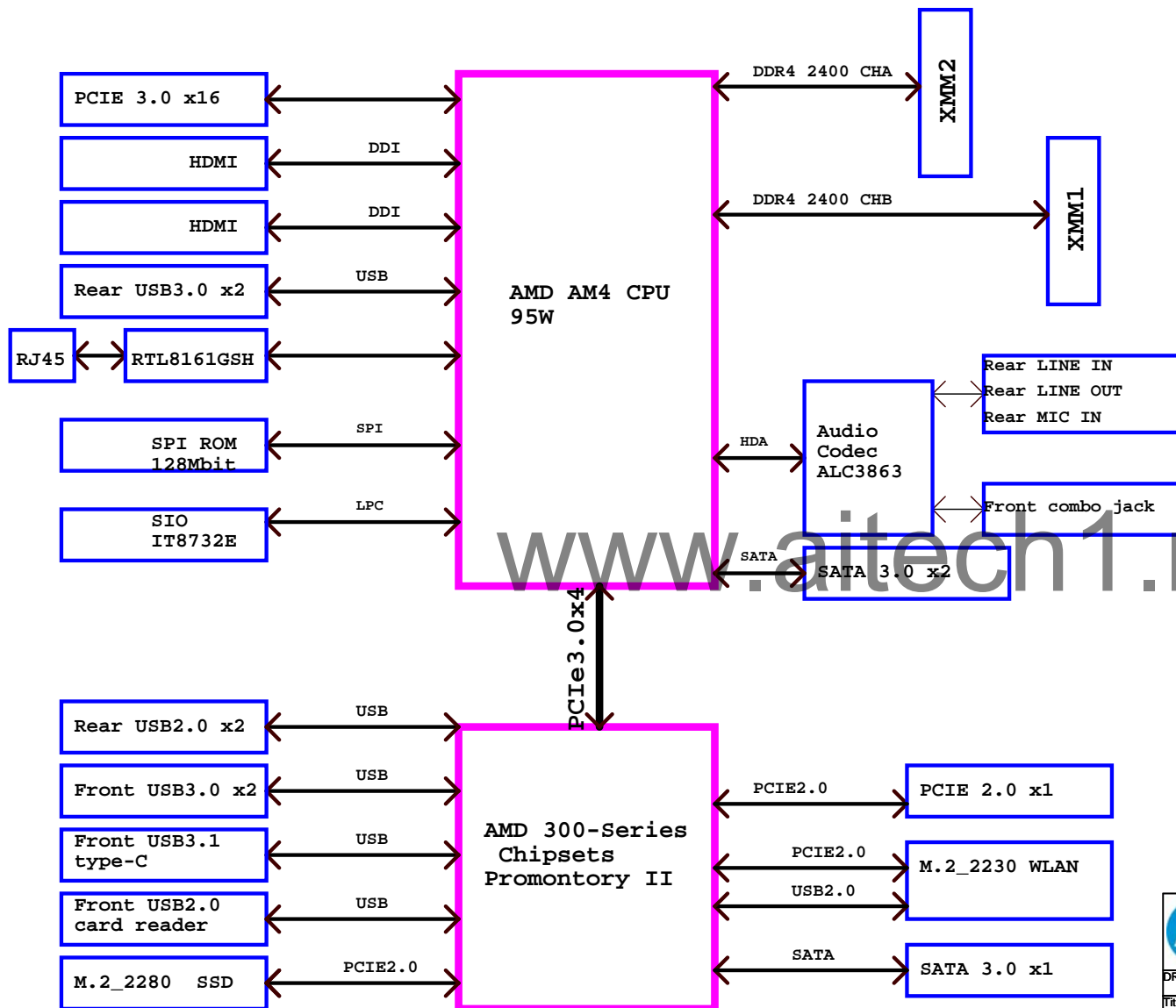
Rev
X2


Date:
Tuesday, June 20, 2017

Sheet
1

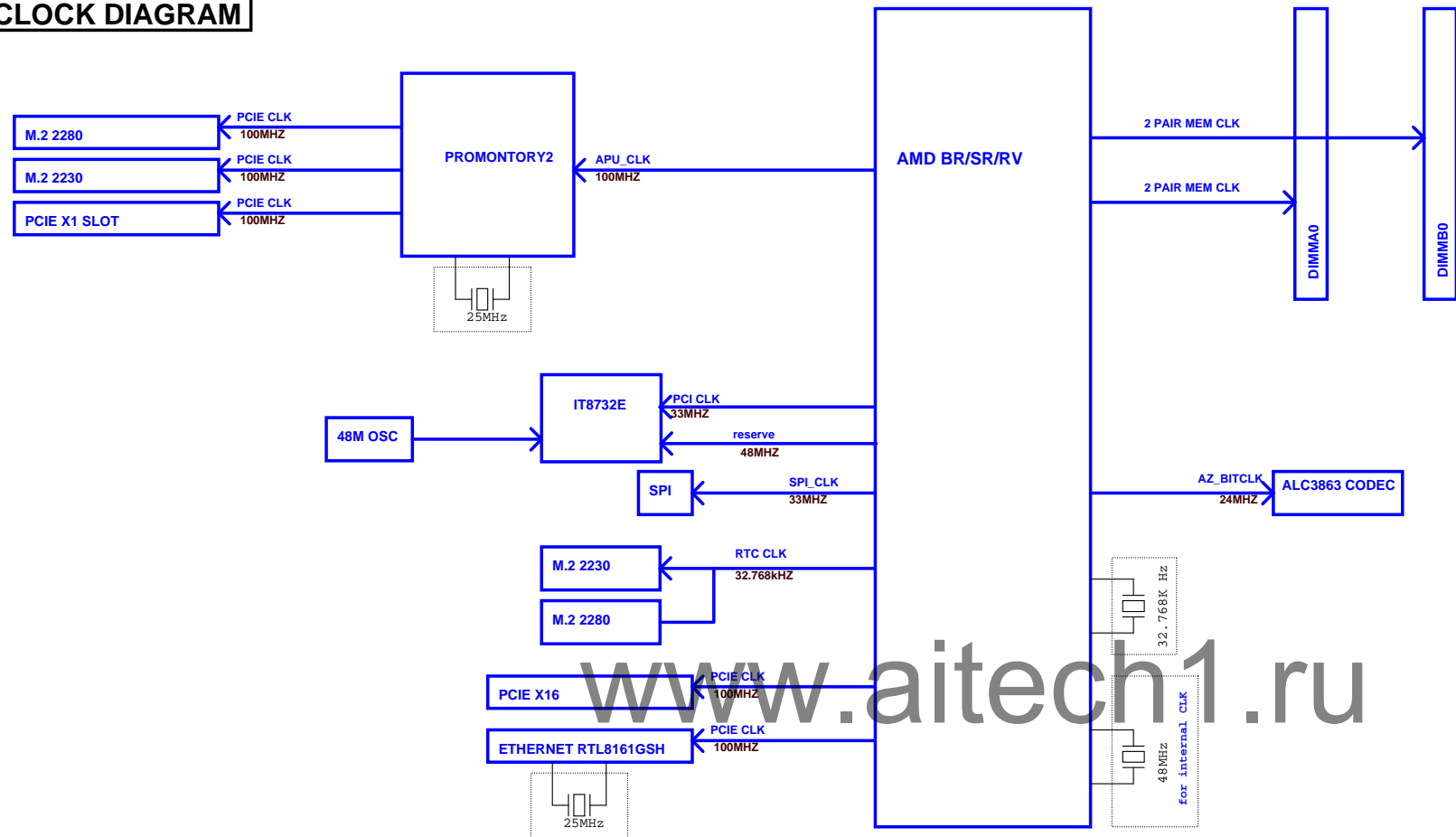
of
68

System BLOCK Diagram

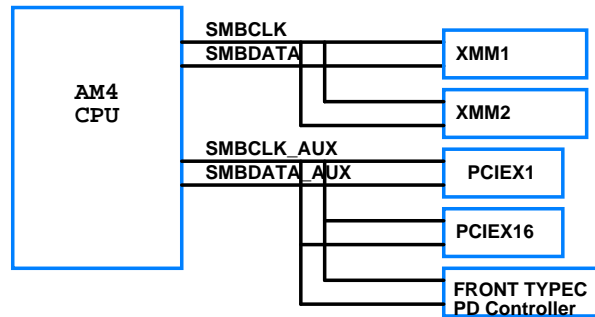


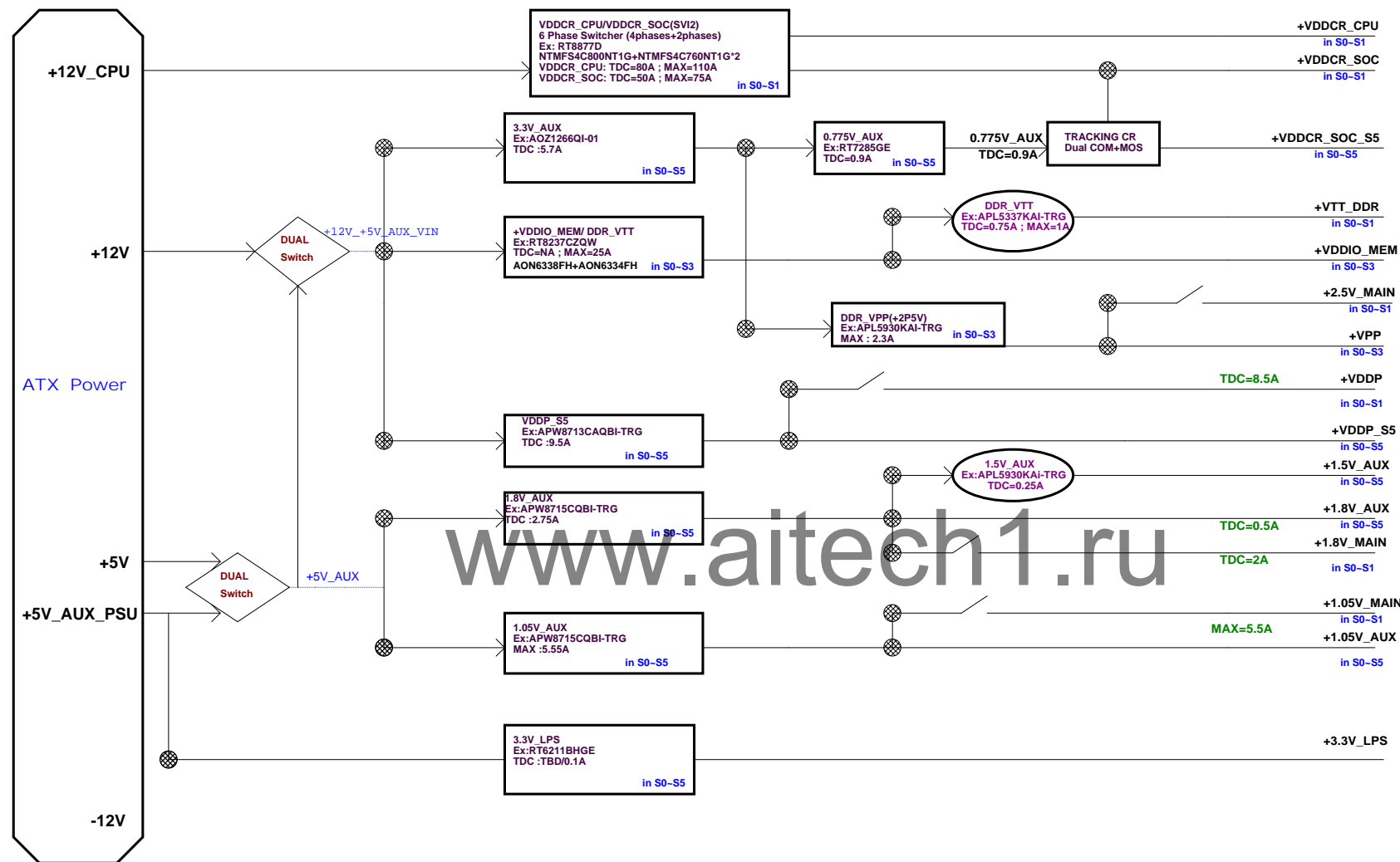
		HP RESTRICTED (HP RESTRICTED SECRET)	
THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.			
DRAWN BY		FOXCONN	
Title		BLOCK DIAGRAM	
Size B	Document Number 921822-000	Rev	X2
Date: Tuesday, June 20, 2017	Sheet 2	of	68

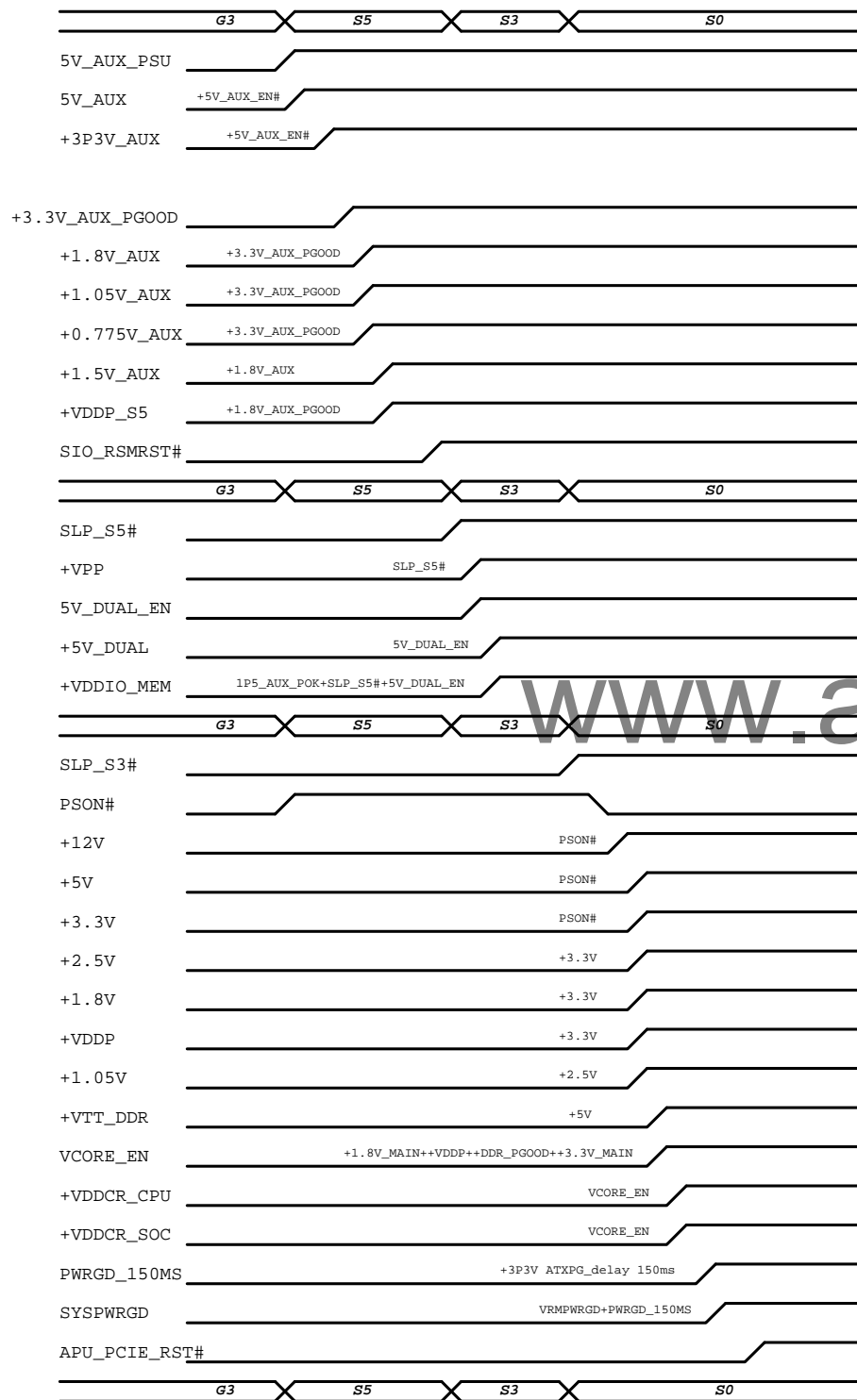
CLOCK DIAGRAM



SM Bus MAP







Promontory Power Sequence

Figure 7 shows the power up and power down sequence.

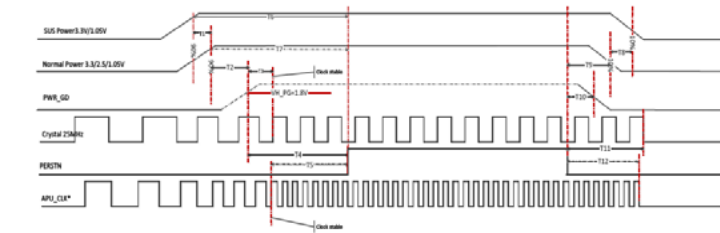
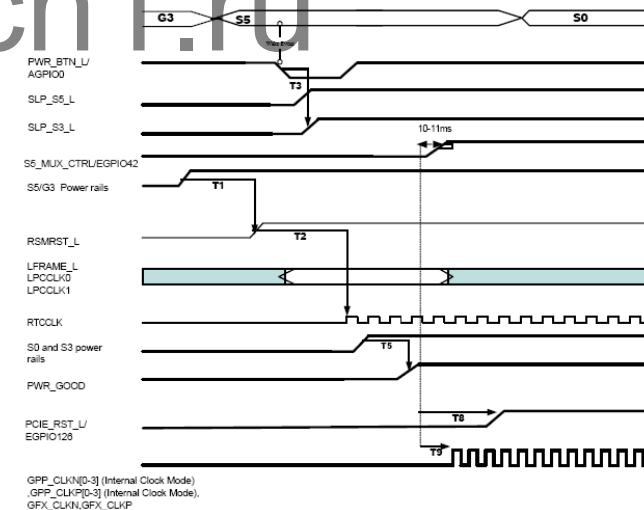


Table 17. Power Sequence Timing

Symbol	Minimum	Maximum	Description
T1	20 ms	–	Suspend power to normal power
T2	10 ms	–	Normal power to PWR_GD asserted
T3	–	2 ms	PWR_GD asserted to crystal stable
T4	40 ms	–	PWR_GD asserted to RESETN deasserted
T5	100 μs	–	APU_CLK stable to RESETN deasserted
T6	70 ms	–	Suspend power to PERSTN deasserted
T7	50 ms	–	Normal power to PERSTN deasserted
T8	1 μs	–	Normal power off to suspend power off
T9	1 μs	–	PERSTN asserted to normal power off
T10	1 μs	–	PERSTN asserted to PWR_GD deasserted
T11	0 μs	–	PERSTN asserted to crystal off
T12	0 μs	–	PERSTN asserted to APU clock off
T13	200 μs	–	PERSTN to GPP_RSTN delay



APU GPIO TABLE

GPIO Pin Name	Power Well	Default Voltage	Mux Function	Default Status	Actual Power Well	Actual Voltage	Usage(BIOS CHECK)	Native or GPIO	BootSet (BIOS Check)
AGPIO0	S5	3.3V	PWR_BTN_R	Native	PU 10K to DEEP S5	+3.3V_LPS	PWRBTN_OUT#		
AGPIO1	S5	3.3V	SYS_RESET#	Native	PU 10K to S5	+3.3V_AUX	SYS_RST#		
AGPIO2	S5	3.3V	WAKE_L	Native	PU 10K to S5	+3.3V_AUX	PCI_EXP_WAKE#		
AGPIO3	S5	3.3V	NA	GPI	PU 10K to S5	+3.3V_AUX	AGPIO3	Strap pin	
AGPIO4	S5	3.3V	NA	GPI	PU 10K to S5	+3.3V_AUX	HP_TYPE_C_INT#		High: No TypeC I2C Interrupt Low: TypeC I2C Interrupt
AGPIO5	S5	3.3V	DEVS_LP0	GPI	Reserve PU 10K to S5	+3.3V_AUX	AGPIO5		
AGPIO6	S5	3.3V	NA	GPI	PD 100K	NA	ME_DiS#	GPO	High: ME Enable Low: ME Disable
AGPIO8	S5	3.3V	NA	GPI	Reserve PU 10K to S5	+3.3V_AUX	NA		
AGPIO9	S5	3.3V	SGPIO0_DATAOUT	GPI	PU 8.2K to S5	+3.3V_AUX	NA		
AGPIO10	S5	3.3V	SDA3_GPIO/SGPIO0_CLK	Native:SDA3_GPIO	PU 2.2K to S5	+3.3V_AUX	SDA3_GPIO		
AGPIO11	S5	3.3V	BLINK	GPI	PD 100K	NA	FLASH_OVERRIDE#	GPI	High: Enable Flash Descriptor Security Override Low: Disable Flash Descriptor Security Override
AGPIO16	S5	3.3V	USB_OC0_L	Native	PU 10K to S5	+3.3V_AUX	USB3_OC_REAR#_SW		
AGPIO17	S5	3.3V	USB_OC1_L/UTDI	Native:USB_OC1_L	Reserve PU 10K to S5	+3.3V_AUX	NA		
AGPIO18	S5	3.3V	USB_OC2_L/UTCK	Native:USB_OC2_L	PU 10K to S5	+3.3V	USB_OC_LAN#_SW		
AGPIO19	S5	3.3V	SCL1/I2C3_SCL	Native:SCL1	PU 2.2K to S5	+3.3V_AUX	SMBCLK_AUX		
AGPIO20	S5	3.3V	SDA1/I2C3_SDA	Native:SDA1	PU 2.2K to S5	+3.3V_AUX	SMBDATA_AUX		
AGPIO21	S5	3.3V	LPC_PD_L	Native	NA	NA	NA		
AGPIO22	S5	3.3V	LPC_PME_L	Native	PU 10K to S5	+3.3V_AUX	LPC_PME_L		
AGPIO23	S5	3.3V	SGPIO0_LOAD	GPI	PU 8.2K to S5	+3.3V_AUX	AGPIO23		
AGPIO24	S5	3.3V	USB_OC3_L/UTDO	Native:USB_OC3_L	PU 8.2K to S5	+3.3V_AUX	SIO_SM#	GPI	High: No SMI Interrupt Low: SMI interrupt
AGPIO40	S5	3.3V	SGPIO0_DATAIN	GPI	NA	NA	NA		
AGPIO78	S0	3.3V	SPI_TFM_CS_L	GPI	NA	NA	NA		
AGPIO84	S0	3.3V	FANIN0	Native	PU 10K to S0	+3.3V	CLR_PSWD#	GPI	High: Not Clear password Low: Clear password
AGPIO85	S0	3.3V	FANOUT0	GPI	PU 10K to S0	+3.3V	CLR_CMOS#	GPI	High: Not Clear CMOS Low: Clear CMOS
AGPIO86	S0	3.3V	NA	GPI	NA	NA	PM_SM#		
AGPIO87	S0	3.3V	SERIRQ	Native	PU 10K to S0	+3.3V	SER_IRQ		
AGPIO88	S0	3.3V	LPC_CLKRUN_L	Native	NA	NA	NA		
AGPIO89	S0	3.3V	GENINT1_L	GPI	Reserve PU 8.2K to S5 Reserve PD 10K	+3.3V	NA		
AGPIO90	S0	3.3V	GENINT2_L	Native	NA	NA	NA		
AGPIO91	S0	3.3V	SPKR	GPI	NA	NA	SPKR		
AGPIO92	S0	3.3V	CLK_REQ0_L/SATA150_L	Native:CLK_REQ0_L	NA	NA	NA		
AGPIO115	S0	3.3V	CLK_REQ1_L	Native	PU 10K to S0	+3.3V	CLK_REQ1		
AGPIO116	S0	3.3V	CLK_REQ2_L	Native	PU 10K to S0	+3.3V	CLK_REQ2		
AGPIO130	S0	3.3V	SATA_ACT_L	Native	PU 10K to S0	+3.3V	SATA_LED#		
EGPIO25	S5	3.3V	PCI_E_RST_L	Native	PU 10K to S5	+3.3V_AUX	APU_PCIE_RST#		
EGPIO42	S5	3.3V	APU_S5_MUX_CTRL	Native	PU 100K to S5	+3.3V_AUX	APU_S5_MUX_CTRL		
EGPIO70	S0	3.3V	NA	GPI	PU 10K to S0	+3.3V	BOOT_BLOCK_REC#	GPI	High: Not Boot Block Recovery Low: Boot Block Recovery
EGPIO74	S0	3.3V	LPCCLK0	Native	PD 2K	NA	CLK_SIO_33MHz	Strap pin	
EGPIO75	S0	3.3V	LPCCLK1	Native	PU 10K to S0	+3.3V	CLK_LPC_33MHz	Strap pin	
EGPIO95	S0	3.3V	NA	GPI	PD 10K	NA	BRD_REV0	GPI	Board Reserve ID BIT0
EGPIO96	S0	3.3V	NA	GPI	PD 10K	NA	BRD_REV1	GPI	Board Reserve ID BIT1
EGPIO97	S0	3.3V	NA	GPI	Reserve PU 10K to S0 Reserve PD 10K	+3.3V	BRD_ID0	GPI	board reversion ID bit 0
EGPIO98	S0	3.3V	NA	GPI	Reserve PU 10K to S0 Reserve PD 10K	+3.3V	BRD_ID1	GPI	board reversion ID bit 1
EGPIO99	S0	3.3V	NA	GPI	Reserve PU 10K to S0 Reserve PD 10K	+3.3V	BRD_ID2	GPI	board reversion ID bit 2
EGPIO100	S0	3.3V	NA	GPI	Reserve PU 10K to S0 Reserve PD 10K	+3.3V	BRD_ID3	GPI	board reversion ID bit 3
EGPIO104	S0	3.3V	LAD0	Native	PU 10K to S0	+3.3V	LPC_AD0		
EGPIO105	S0	3.3V	LAD1	Native	PU 10K to S0	+3.3V	LPC_AD1		
EGPIO106	S0	3.3V	LAD2	Native	PU 10K to S0	+3.3V	LPC_AD2		
EGPIO107	S0	3.3V	LAD3	Native	PU 10K to S0	+3.3V	LPC_AD3		
EGPIO108	S0	3.3V	ESPI_ALERT_L/LDRQ0_L	Native:LDRQ0_L	NA	NA	NA		
EGPIO109	S0	3.3V	LFRAME_L	Native	NA	NA	APU_LFRAME#		
EGPIO113	S0	3.3V	SCL0/I2C2_SCL	Native:SCL0	PU 2.2K to S0	+3.3V	SMBCLK_MAIN		
EGPIO114	S0	3.3V	SDA0/I2C2_SDA	Native:SDA0	PU 2.2K to S0	+3.3V	SMBDATA_MAIN		
EGPIO117	S0	3.3V	SPI_CLK/ESPI_CLK	Native:SPI_CLK	PU 10K to S0	+1.8V	APU_SPI_CLK		
EGPIO118	S0	3.3V	SPI_CS1_L	Native	PU 10K to S0	+1.8V	APU_SPI_CS#		
EGPIO119	S0	3.3V	SPI_CS2_LESPI_CS_L	Native:SPI_CS2_L	NA	NA	NA		
EGPIO122	S0	3.3V	SPI_WP_LESPI_DAT2	GPI	Reserve PU 10K to S0	+1.8V	APU_SPI_I02		
EGPIO131	S0	3.3V	CLK_REQ3_L/SATA151_L	Native:CLK_REQ3_L	NA	NA	NA		
EGPIO132	S0	3.3V	CLK_REQ0_L/OSCIN	Native:CLK_REQ0_L	PU 10K to S0	+3.3V	CLK_REQ0#		
EGPIO133	S0	3.3V	SPI_HOLD_LESPI_DAT3	GPI	Reserve PU 10K to S0	+1.8V	APU_SPI_I03		

PCH GPIO TABLE

GPIO Pin Name	Power Well	Default Voltage	Mux Function	Default Status	Actual Power Well	Actual Voltage	Usage(BIOS CHECK)	Native or GPIO	BootSet (BIOS Check)
GPIO_R0	VCC33	3.3V	NA		NA	NA	NA		
GPIO_R1	VCC33	3.3V	NA		NA	NA	NA		
GPIO_R2	VCC33	3.3V	NA		NA	NA	NA		
GPIO_R3	VCC33	3.3V	NA		NA	NA	NA		
GPIO_R4	VCC33	3.3V	DEBUG32		PU 200K to S0	+3.3V	GPIOR4		
GPIO_R5	VCC33	3.3V	DEBUG33		PU 1K	NA	GPIOR5		
GPIO_R6	VCC33	3.3V	DEBUG34		PU 200K to S0	+3.3V	GPIOR6		
GPIO_R7	VCC33	3.3V	DEBUG25		PU 200K to S0	+3.3V	GPIOR7		
GPIO_R8	VCC33	3.3V	DEBUG25		PU 200K to S0	+3.3V	GPIOR8		
GPIO_R9	VCC33	3.3V	DEBUG27		PU 200K to S0	+3.3V	GPIOR9		
GPIO_R10	VCC33	3.3V	DEBUG28		NA	NA	NA		
GPIO_R11	VCC33	3.3V	DEBUG29		PU 200K to S0	+3.3V	GPIOR11		
GPIO_R12	VCC33	3.3V	DEBUG30		NA	NA	NA		
GPIO_R13	VCC33	3.3V	DEBUG31		NA	NA	NA		
GPIO_R14	VCC33	3.3V	DEBUG37		NA	NA	NA		
GPIO0	VCC33	3.3V	NA		NA	NA	M2_2230_DET#	GPI	High: M2_2230 device Not detect Low: M2_2230 device detect
GPIO1	VCC33	3.3V	NA		PU 10K to S0	+3.3V	F_AUDIO_DET#	GPI	High: Front AUDIO cable Not detect Low: Front AUDIO cable detect
GPIO2	VCC33	3.3V	NA		PU 10K to S0	+3.3V	FRONT_USB_DET#	GPI	High: Front USB cable Not detect Low: Front USB cable detect
GPIO3	VCC33	3.3V	NA	Reserve PU 10K to S5	+3.3V_AUX	W_DISABLE2#	GPO	High: Wi-Fi active Low: Wi-Fi inactive	
GPIO4	VCC33	3.3V	NA		NA	NA	NA		
GPIO5	VCC33	3.3V	NA		NA	NA	NA		
GPIO6	VCC33	3.3V	NA		PU 10K to S0	+3.3V	CR_USB_DET#	GPI	High: Card Reader cable Not detect
GPIO7	VCC33	3.3V	NA		NA	NA	NA		

SIO GPIO TABLE

Item	Power Plane	Voltage Level	Mux Function	Usage	PULL HIGH/DOWN	Remark	GPIO
GP10	3VSB	3.3V	PCIRST3#	PCIRST3#_SIO	Reserve 10K HIGH +3.3V	PCIE1 RST#/PCIE19 RSTLAN RST#	
GP11	VCC3/3VSB	3.3V	PCIRST2#	NA	NA	NA	
GP12	VCC3/3VSB	3.3V	PCIRST1#	PCIRST1#_SIO	Reserve 10K HIGH +3.3V	M2230 RST#M2230 RST#	
GP13	VCC3/3VSB	3.3V	PWR0K1	NA	NA	NA	
GP14	VCC3/3VSB	3.3V	PCH_C1/VCORE_EN	NA	NA	NA	
GP15	VCC3/3VSB	3.3V	PCIRST1#/CIRT2/CPU_PG	NA	NA	NA	
GP16	VCC3/3VSB	3.3V	5VSB_CTRL/CIRRX2	+5V_AUX_EN#	10K HIGH +5V_AUX_PSU	+5V_AUX_ENABLE	
GP17	VCC3/3VSB	3.3V	R2W#	NA	NA	NA	
GP20	3VSB	3.3V	CTS2#	SIO_GP20_GNRLED	1K HIGH +3.3V_AUX	CONTROL FRONT GREEN LED	GPO
GP21	3VSB	3.3V	DCD2#	SIO_GP21_WLWLED	1K HIGH +3.3V_AUX	CONTROL FRONT YELLOW LED	GPO
GP22	3VSB	3.3V	SCK	SIO_SPI_CLK	4.7K HIGH +3.3V_LPS	SPI_CLK	
GP23	3VSB	3.3V	SI	SIO_SPI_SI	4.7K HIGH +3.3V_LPS	SPI SI I/O	
GP24	3VSB	3.3V	R2S2#	COMM_B_DETECT#	10K HIGH +3.3V_AUX	COM DETECT	GPI
GP25	3VSB	3.3V	DSR2#	NA	1K PD GND	BOOT BLOCK ENABLE	GPI
GP26	3VSB	3.3V	SOLUT2	BOOT_BLOCK_EN#	1K HIGH +3.3V	THERMTRIP DETECT	
GP27	3VSB	3.3V	SIN2	SIO_THERMTRIP#	10K HIGH +3.3V	ATX POWER GOOD	
GP30	VCC3/3VSB	3.3V	ATXPG	PWR0K_PS	100K HIGH +3.3V	CONTROL BLUE LED	GPO
GP31	VCC3/3VSB	3.3V	PWMOUT	SIO_B	NA	NA	
GP32	VCC3/3VSB	3.3V	DPWROK	NA	NA	NA	
GP33	VCC3/3VSB	3.3V	SUSACK#	NA	NA	NA	
GP34	VCC3/3VSB	3.3V	SUSWAKE#	NA	NA	NA	
GP35	VCC3/3VSB	3.3V	FAN_TAC4	SIO_G	100K HIGH +3.3V	CONTROL GREEN LED	GPO
GP36	VCC3/3VSB	3.3V	FAN_CTL3	SIO_R	100K HIGH +3.3V	CONTROL RED LED	GPO
GP37	VCC3/3VSB	3.3V	FAN_TAC3	NA	NA	NA	
GP40	3VSB	3.3V	3VSSW#	3VSSW#	Reserve 4.7K HIGH +3.3V_LPS	5V_DUAL_USB_EN	
GP41	3VSB	3.3V	PWR0K2	PWR0K2_140MS	1K HIGH +3.3V	PWR0K2_140MS SIGNAL	
GP42	3VSB	3.3V	FANIN#	PF0IN#	2.2K HIGH +5V_AUX_PSU	MAIN POWER CONTROL	
GP43	3VSB	3.3V	PANW#	PWR0K1#	10K HIGH +3.3V_LPS	POWER BUTTON IN	
GP44	3VSB	3.3V	PWRON#	PWRON#_OUT#	10K HIGH +3.3V_LPS	POWER BUTTON OUT	
GP48	3VSB	3.3V	D_RX0/SMCLK2	SIO_SM#	8.2K HIGH +3.3V_AUX	Reserve for SMI	GPO
GP47	VCC3/3VSB	3.3V	D_TX0/SMDAT2	NA	NA	NA	
GP50	VCC3/3VSB	3.3V	SO	SIO_SPI_SO	4.7K HIGH +3.3V_LPS	SPI SO I/O	
GP51	VCC3/3VSB	3.3V	FAN_CTL2	SYS_FAN_PWA2	1K HIGH +3.3V	DETECT SYSTEM FAN SPEED	
GP52	VCC3/3VSB	3.3V	FAN_TAC2	SYS_FAN_TACH2	10K HIGH +3.3V	CONTROL SYSTEM FAN SPEED	
GP53	3VSB	3.3V	SUSC#	NA	NA	NA	
GP54	3VSB	3.3V	PWR0K	SIO_PWR0K	10K HIGH +3.3V_AUX	NA	
GP55	3VSB	3.3V	RSMRSTW/CIRRX1	SIO_RSMRST#	10K HIGH +3.3V_AUX	RESUME RESET	
GP56	VCC3/3VSB	3.3V	MCLK	MCLK	4.7K HIGH +5V_DUAL	MOUSE	
GP57	VCC3/3VSB	3.3V	MDAT	MDAT	4.7K HIGH +5V_DUAL	MOUSE	
GP60	VCC3/3VSB	3.3V	KCLK	KCLK	4.7K HIGH +5V_DUAL	KEYBOARD	
GP61	VCC3/3VSB	3.3V	KDAT	KDAT	4.7K HIGH +5V_DUAL	KEYBOARD	
GP62	VCC3/3VSB	3.3V	KRST#	KBRST#	10K HIGH +3.3V	MOSSE AND KEYBOARD RST	
GP63	VCC3/3VSB	3.3V	SLP_SUS#VLDT_EN	NA	NA	NA	
GP70	3VSB	3.3V	KSIO	SIO_GP70	10K HIGH +3.3V	POP_NOISE CONTROL	GPO
GP71	3VSB	3.3V	KS1	NA	NA	NA	
GP72	3VSB	3.3V	KS00/JP1	SIO_JP1	1K HIGH +3.3V_LPS	STRAP PIN	
GP73	3VSB	3.3V	KS01	NA	NA	NA	
GP74	3VSB	3.3V	KS02	SIO_GP74	10K HIGH +3.3V_LPS	KEYBOARD MATRIX SCAN OUTPUT	
GP75	3VSB	3.3V	KS03	SIO_GP75	10K HIGH +3.3V_LPS	KEYBOARD MATRIX SCAN OUTPUT	
GP76	3VSB	3.3V	KS04	NA	NA	NA	
GP77	3VSB	3.3V	KS05	NA	NA	NA	
GP85	3VSB	3.3V	IO_SCIW/SMDAT0	NA	NA	NA	
GP86	3VSB	3.3V	SMCLK0	NA	NA	NA	



HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY

FOXCONN

Title

GPIO TABLE

Size B

Document Number

921822-000

Rev

X2

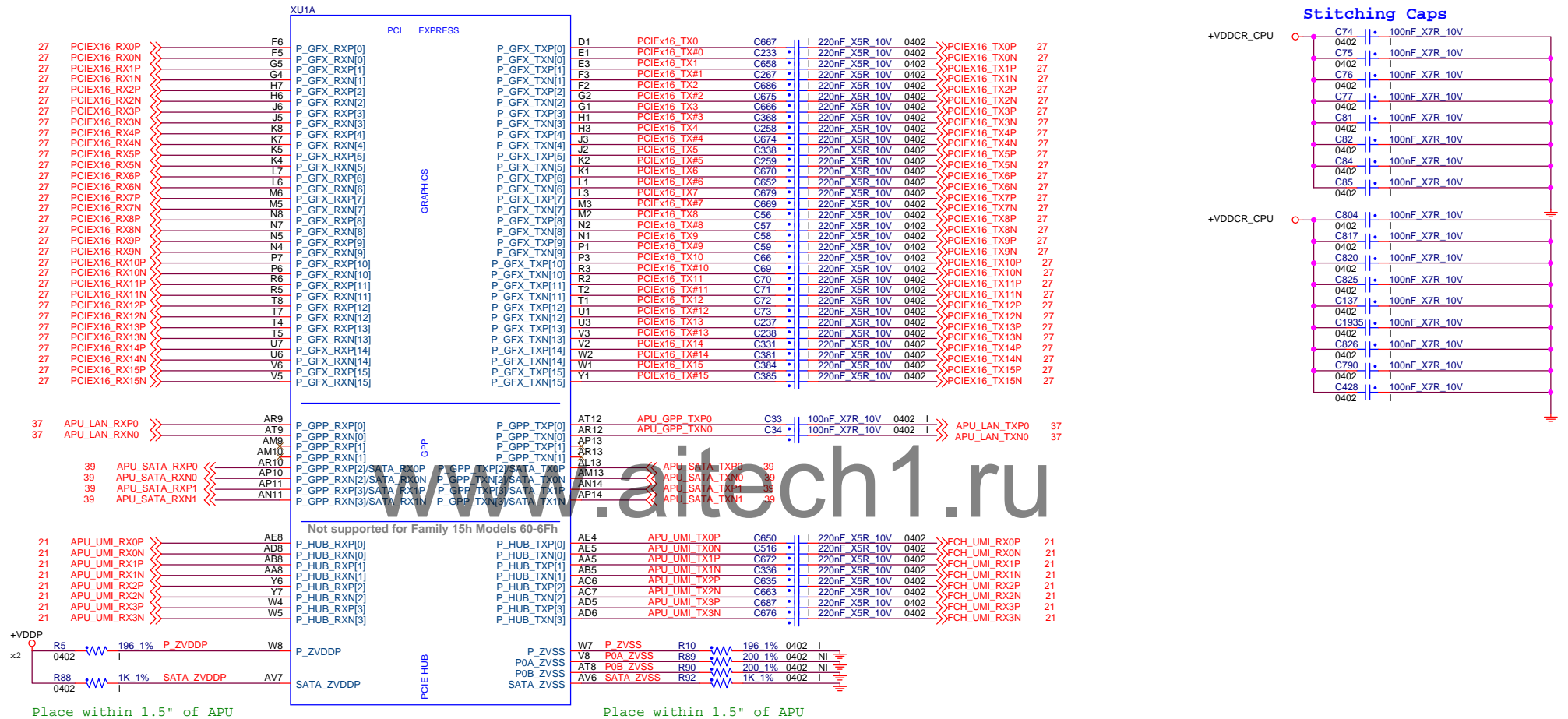
Date: Tuesday, June 20, 2017

Sheet 6 of 68

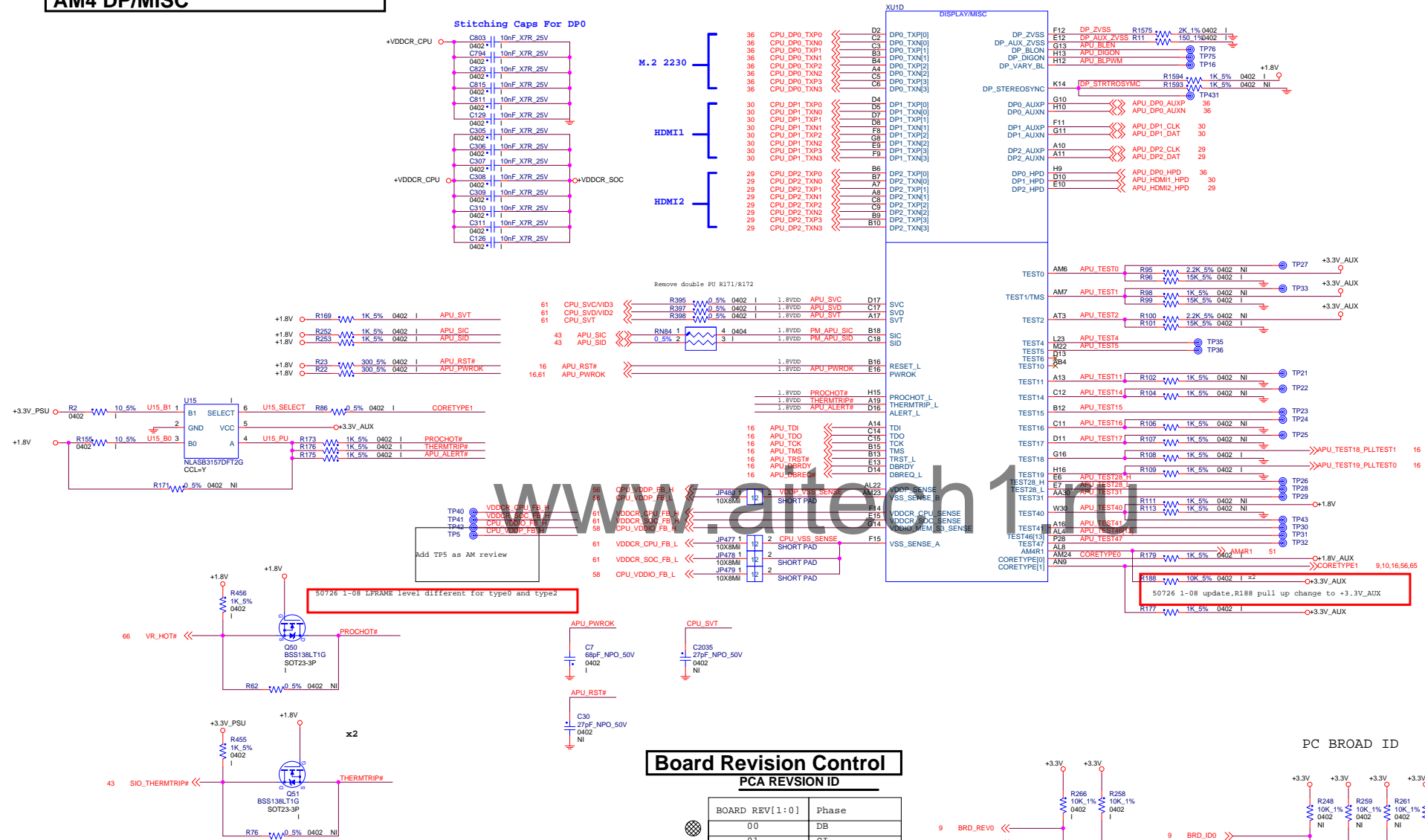
AM4 PCIE Interface

PCIe Gen3: Recommended value is 220-nF 10%. (Range from 176-265nF)
PCIe Gen1 and Gen2: Recommended value is 100-nF 10%. (Range from 75-200nF)

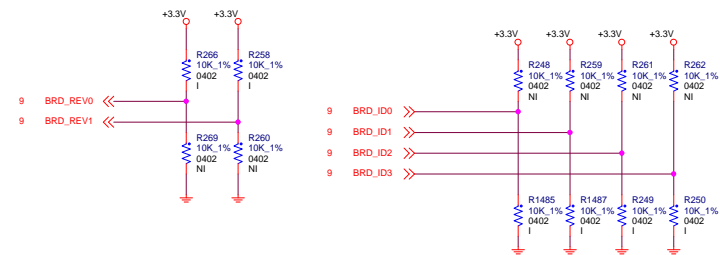
PCIeX16 1st GFX Slot

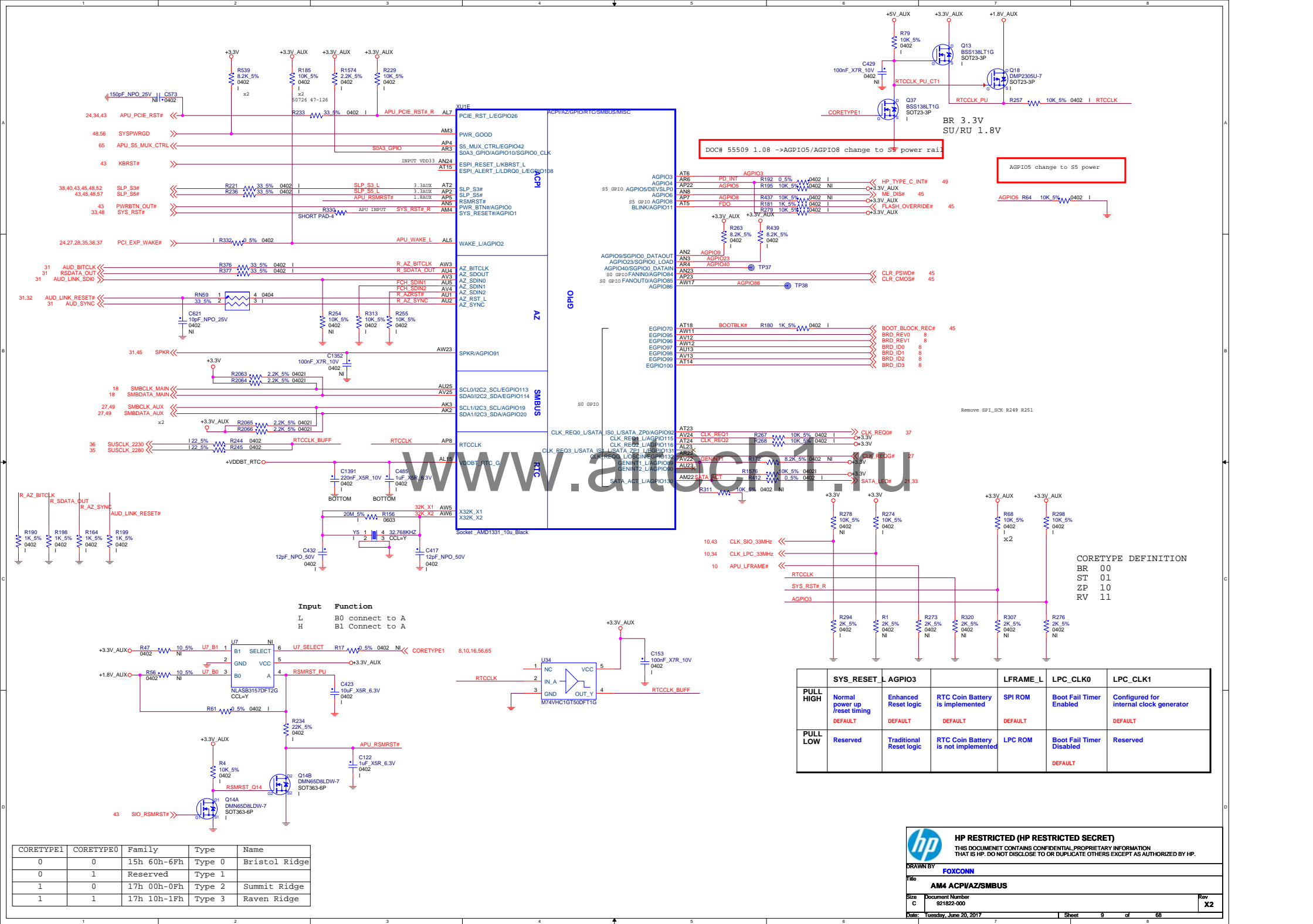


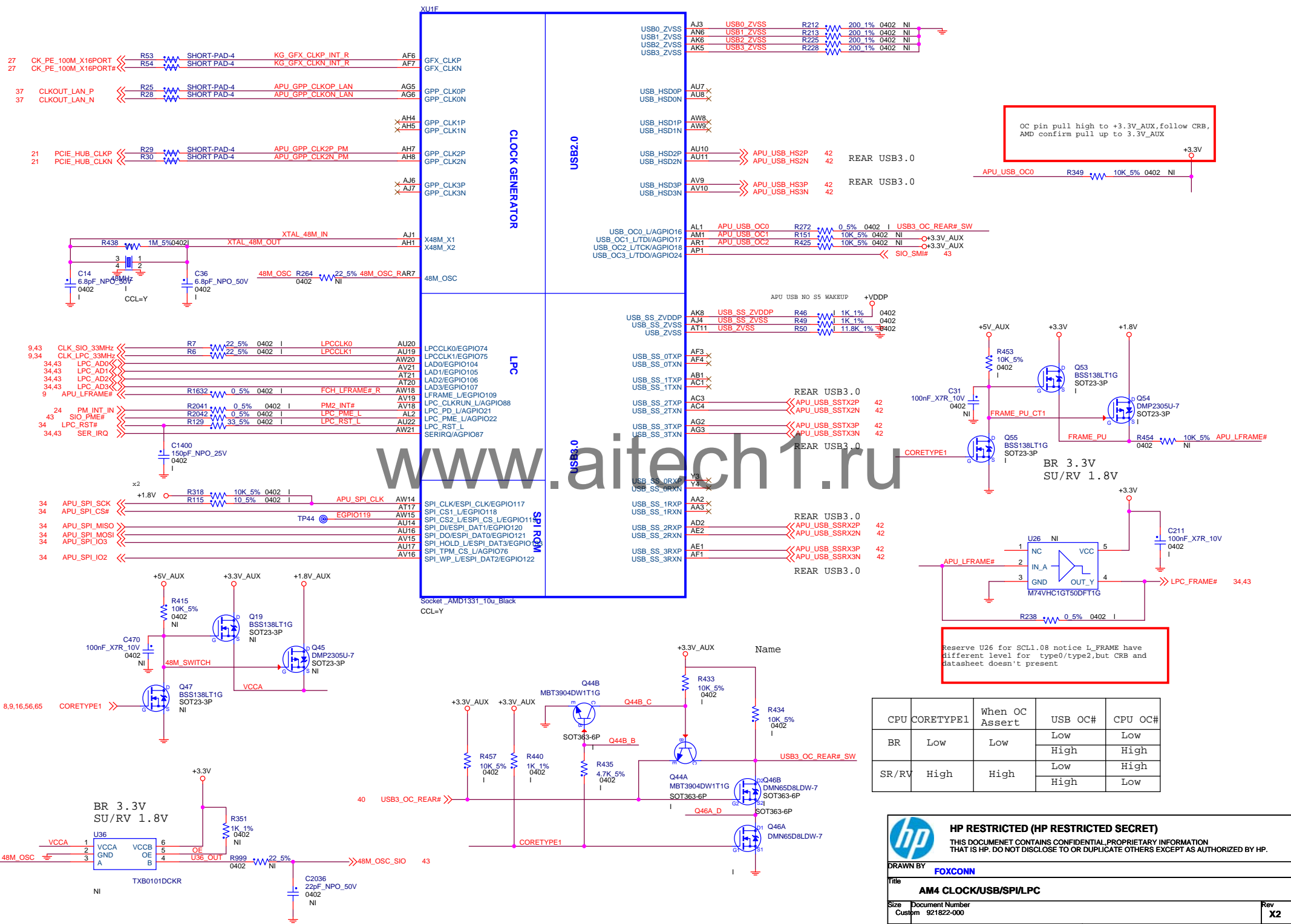
AM4 DP/MISC



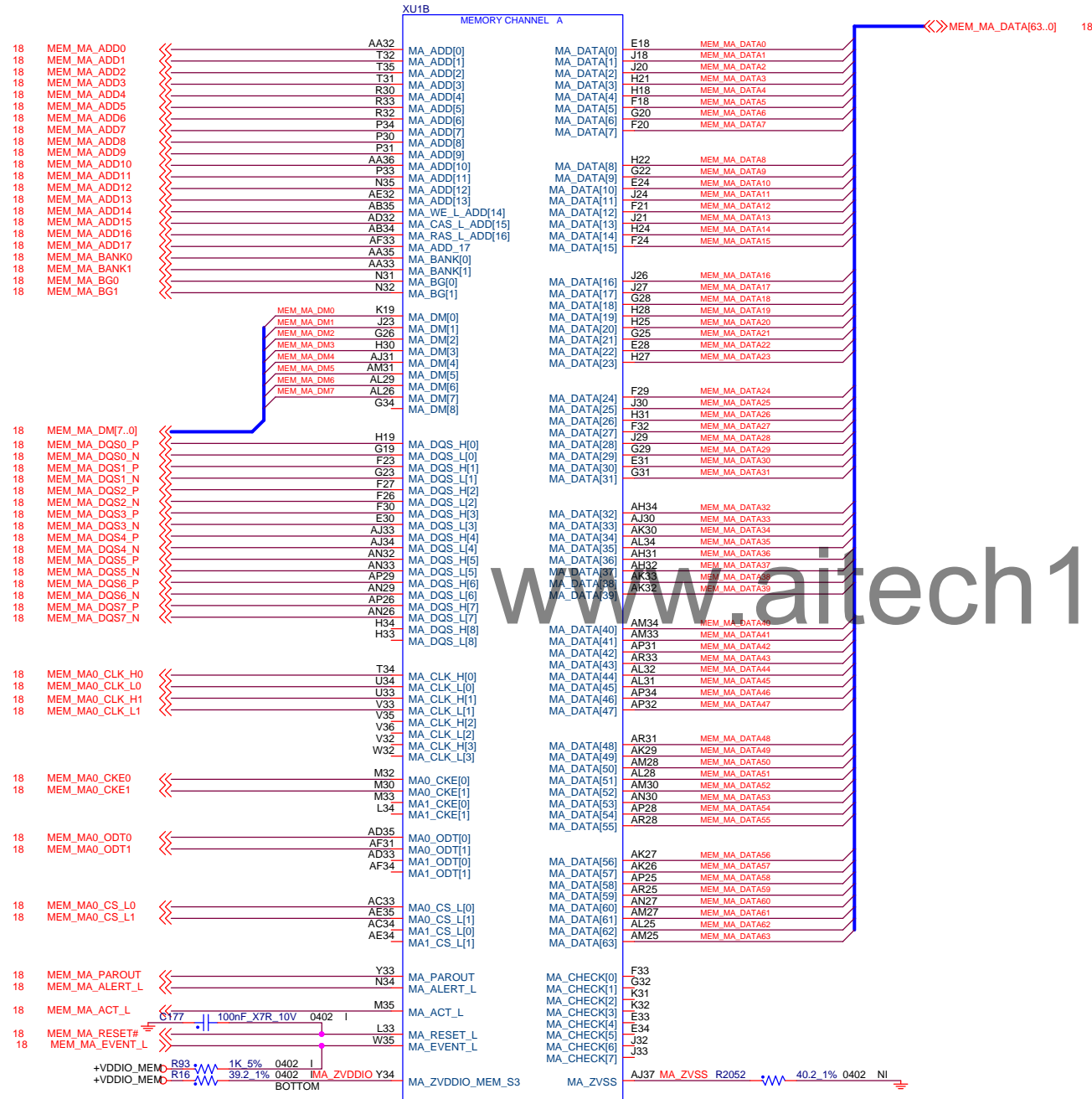
Board Revision Control		
PCA REVISION ID		
BOARD	REV[1:0]	Phase
00		DB
01		SI
10		PV
11		SMVB
00		1st Major ECN
01		2nd Major ECN
10		3rd Major ECN
11		4th Major ECN






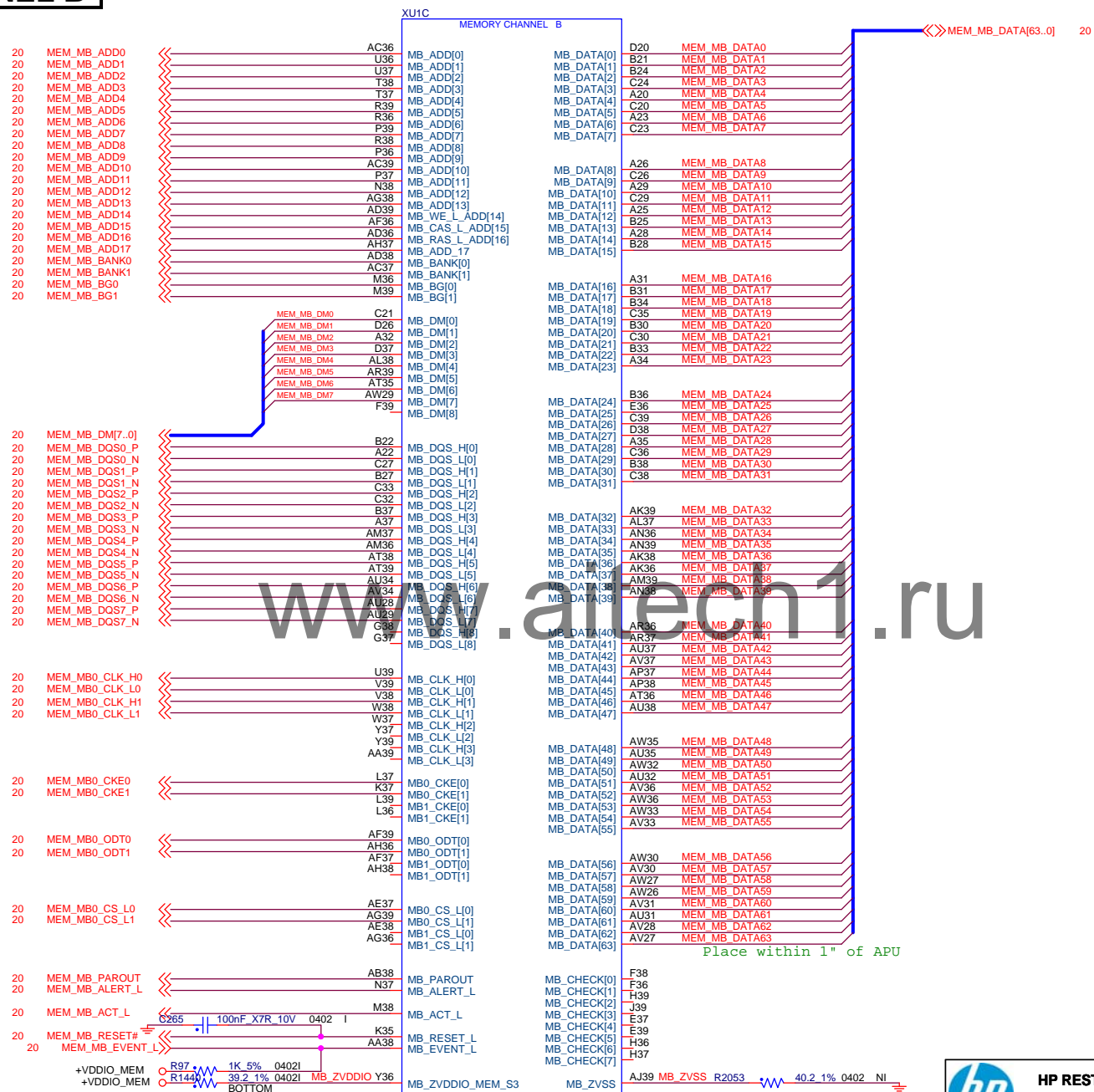


AM4 DDR4 CHANNEL A



Place within 1" of APU

		HP RESTRICTED (HP RESTRICTED SECRET)	
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.			
DRAWN BY FOXCONN			
Title Memory Chanel A			
Size	Document Number	Rev	
Custom	921822-000	X2	
Date:	Tuesday, June 20, 2017	Sheet	11 of 68

FM2+ DDR3 CHANNEL B

HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION
THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY

Y **FOXCONN**

Title

Memory Chanel B

Size	Document Number
Custom	921822-000

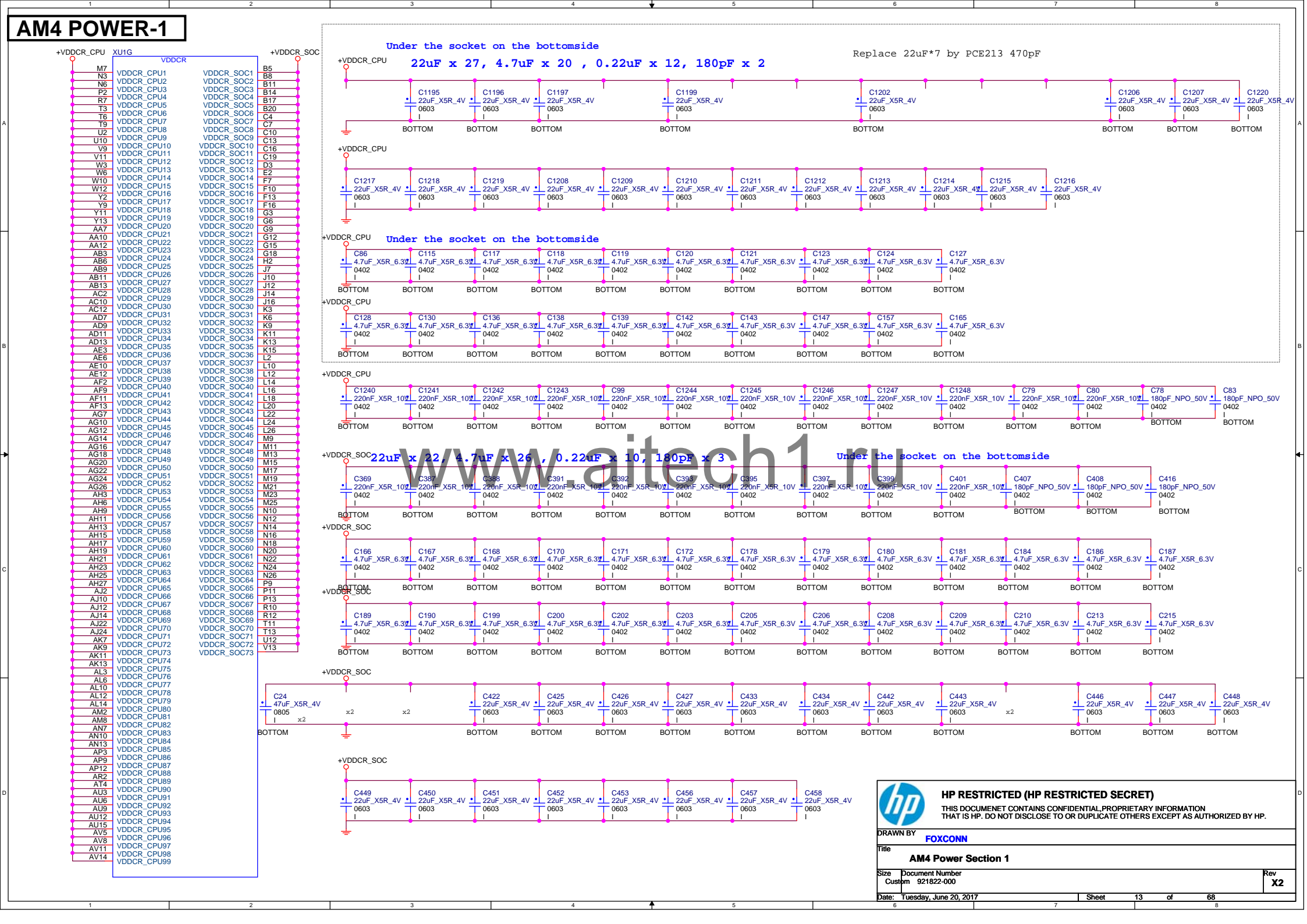
Rev	X2
-----	----

Date: Tuesday, June 20, 2017

Sheet	12	of	68
-------	----	----	----

68

AM4 POWER-1



HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY

FOXCONN

Title

AM4 Power Section 1

Size

Document Number

Custom 921822-000

Rev

X2

Date:

Tuesday, June 20, 2017

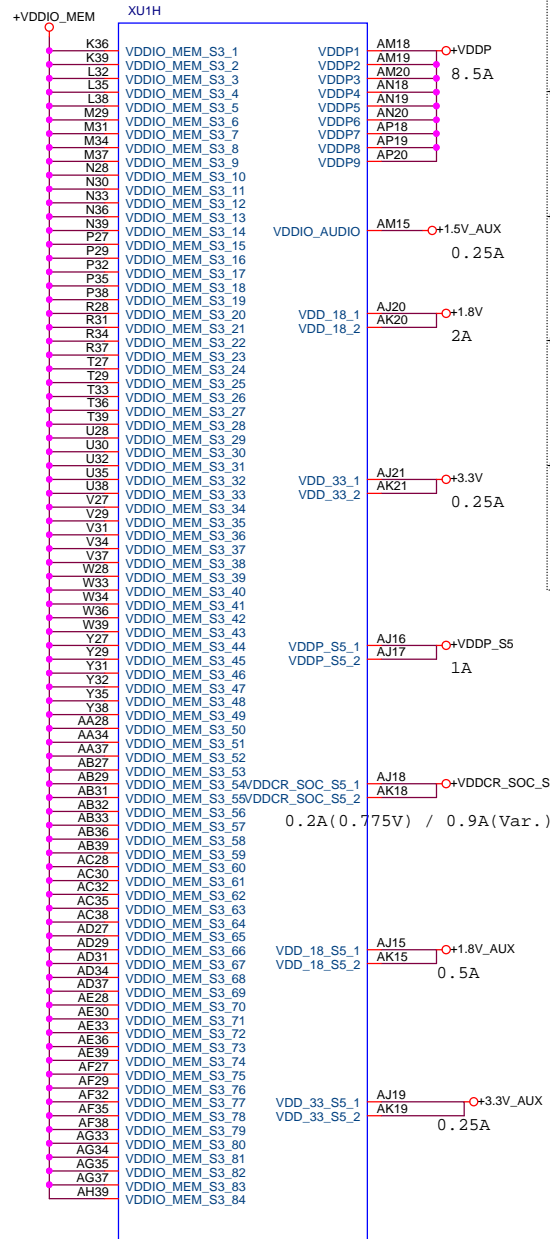
Sheet

13

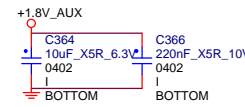
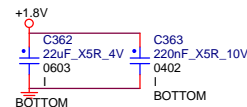
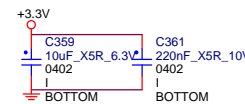
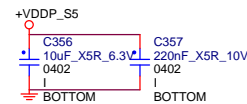
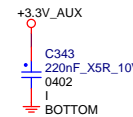
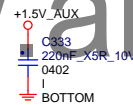
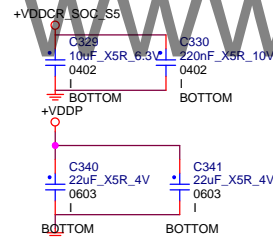
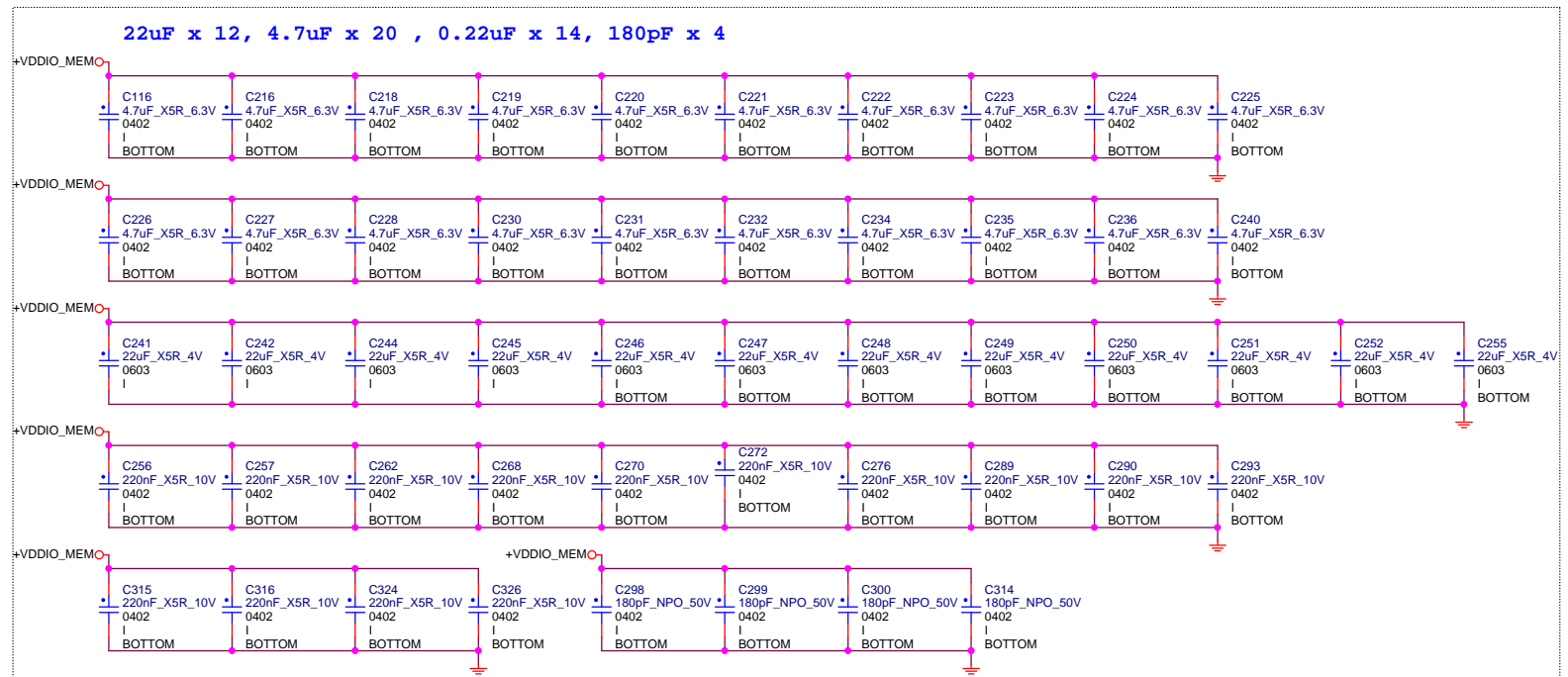
of


68

AM4 POWER-2



Socket_AMD1331_10u_Black



**HP RESTRICTED (HP RESTRICTED SECRET)**
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

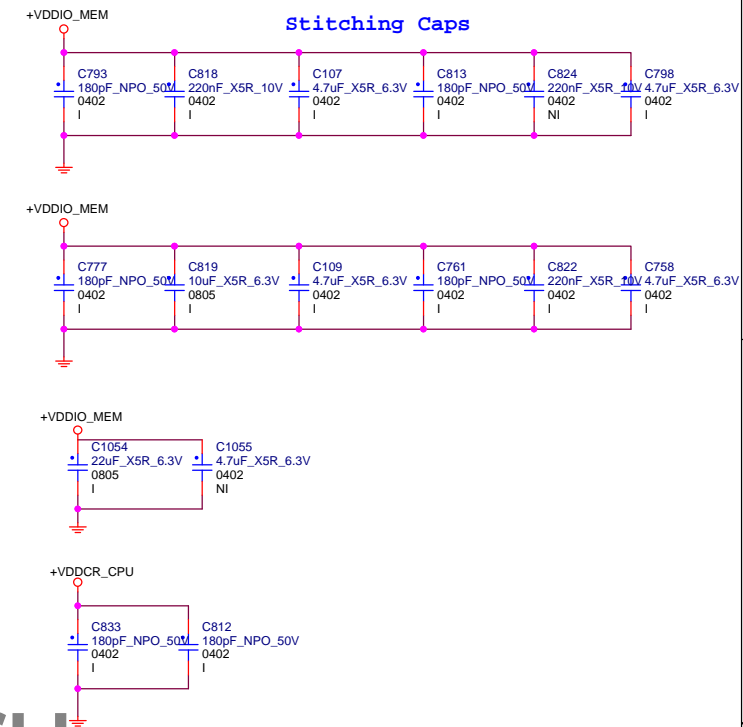
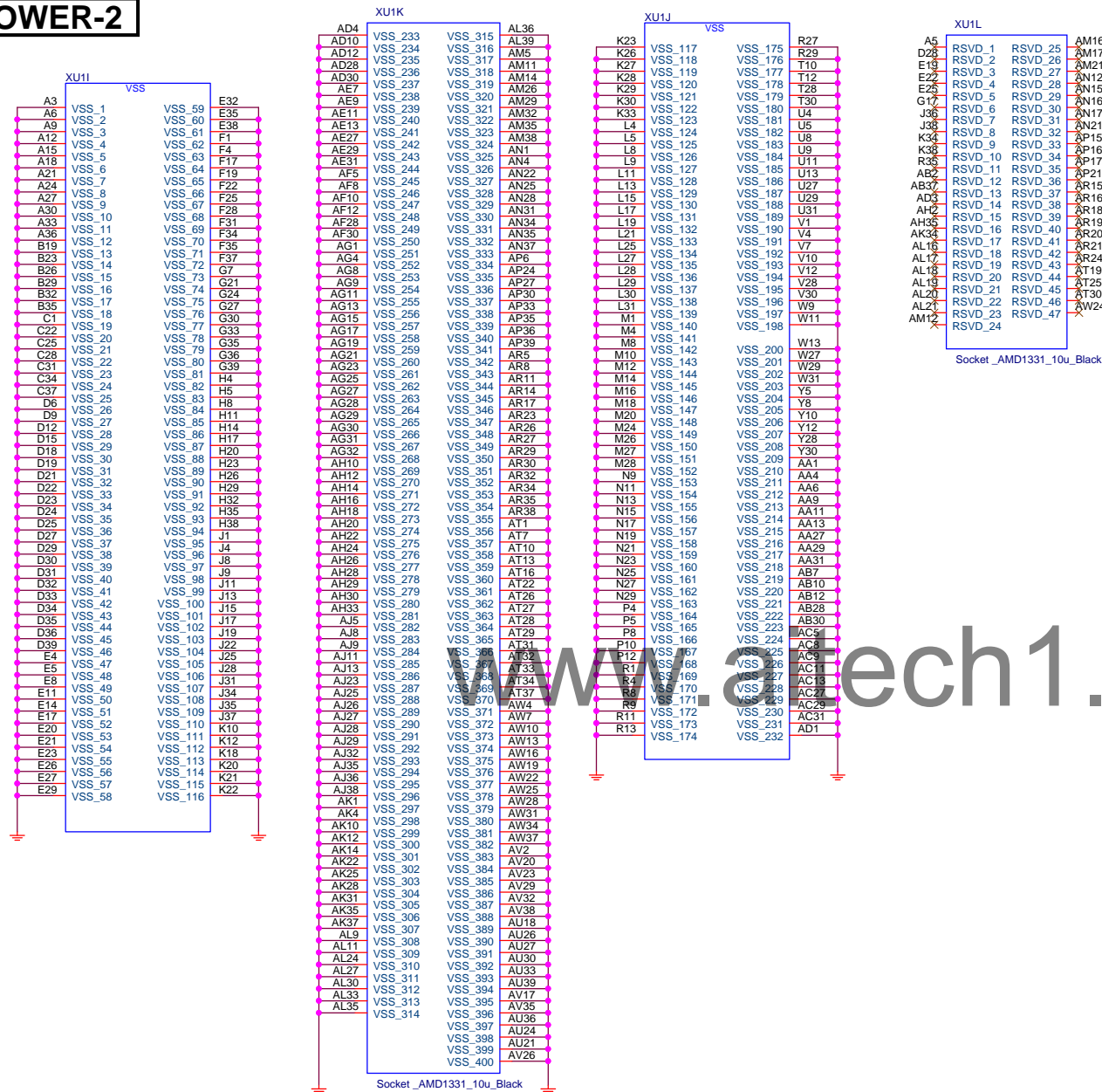
DRAWN BY
FOXCONN

Title
AM4 Power Section 2

Size Custom	Document Number 921822-000	Rev X2
-----------------------	--------------------------------------	------------------

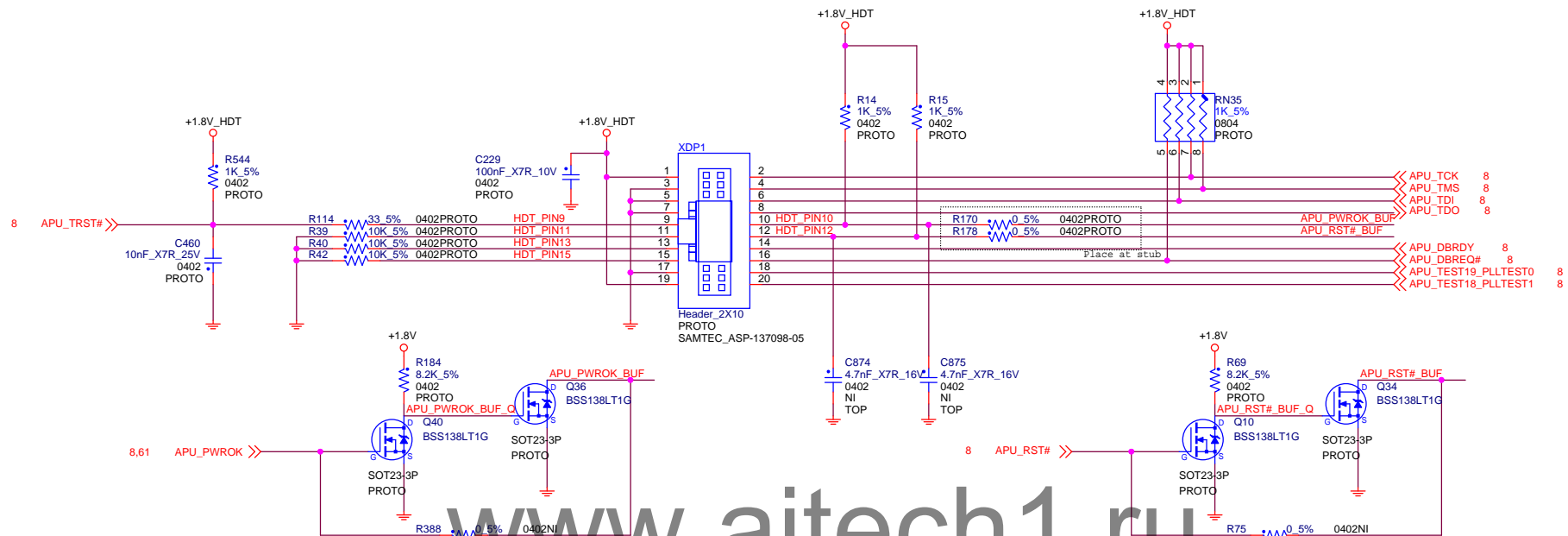
Date: Tuesday, June 20, 2017	Sheet 14 of 68
-------------------------------------	------------------------------

FM2 POWER-2

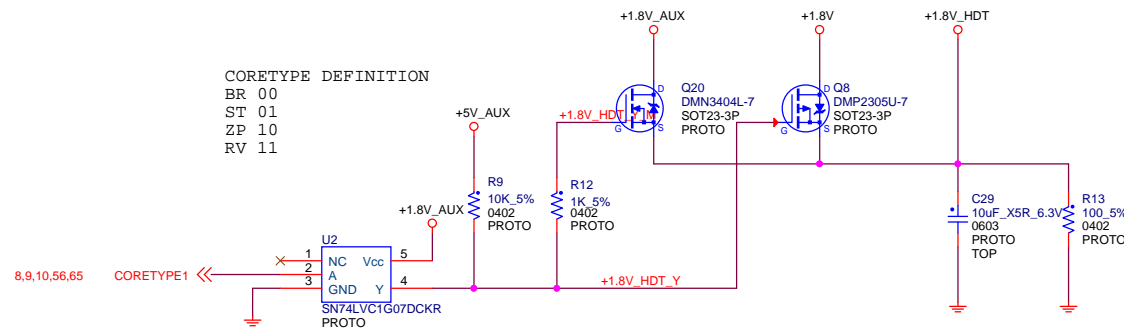


HDT+

All BOM I part in this page are only used for PV
phase debug, will change to PROTO when MP
HDT+ Connector



CORETYPE DEFINITION
BR 00
ST 01
ZP 10
RV 11



HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION
THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY

FOXCONN

Title

System Debug Ports

Size

Document Number

Custom

921822-000

Rev

X2

Date: Tuesday, June 20, 2017

Sheet


16

of

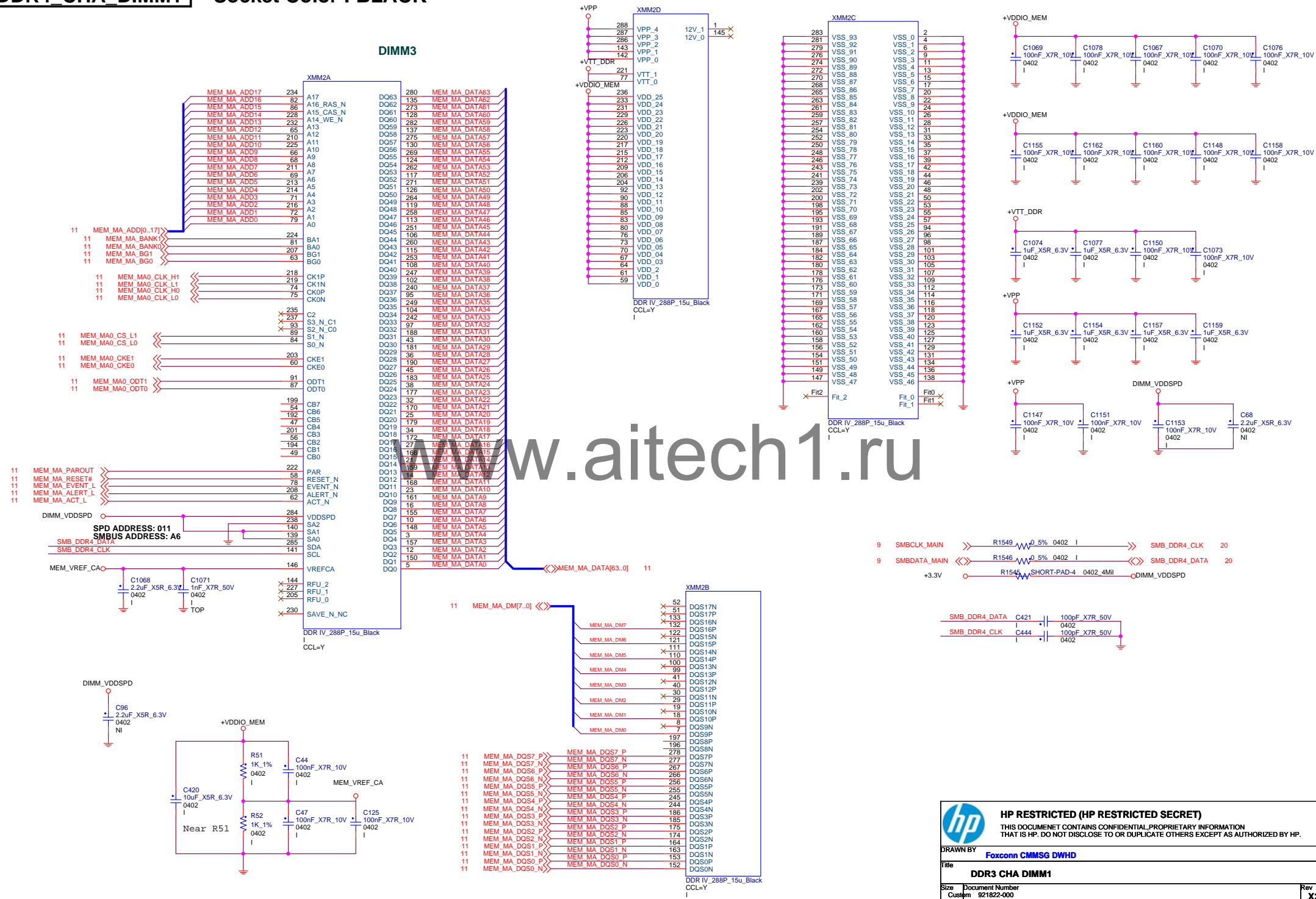
68

www.aitech1.ru


Near R1549

		HP RESTRICTED (HP RESTRICTED SECRET)	
		THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
DRAWN BY		Foxconn CMMSG DWHD	
Title		DDR3 CHA DIMM0	
Size	Document Number	Rev X2	
Custom	921822-000		
Date: Tuesday, June 20, 2017		Sheet	17 of 68

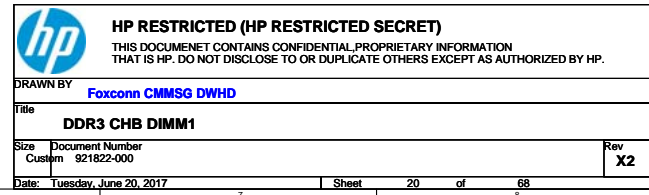
Socket Color : BLACK

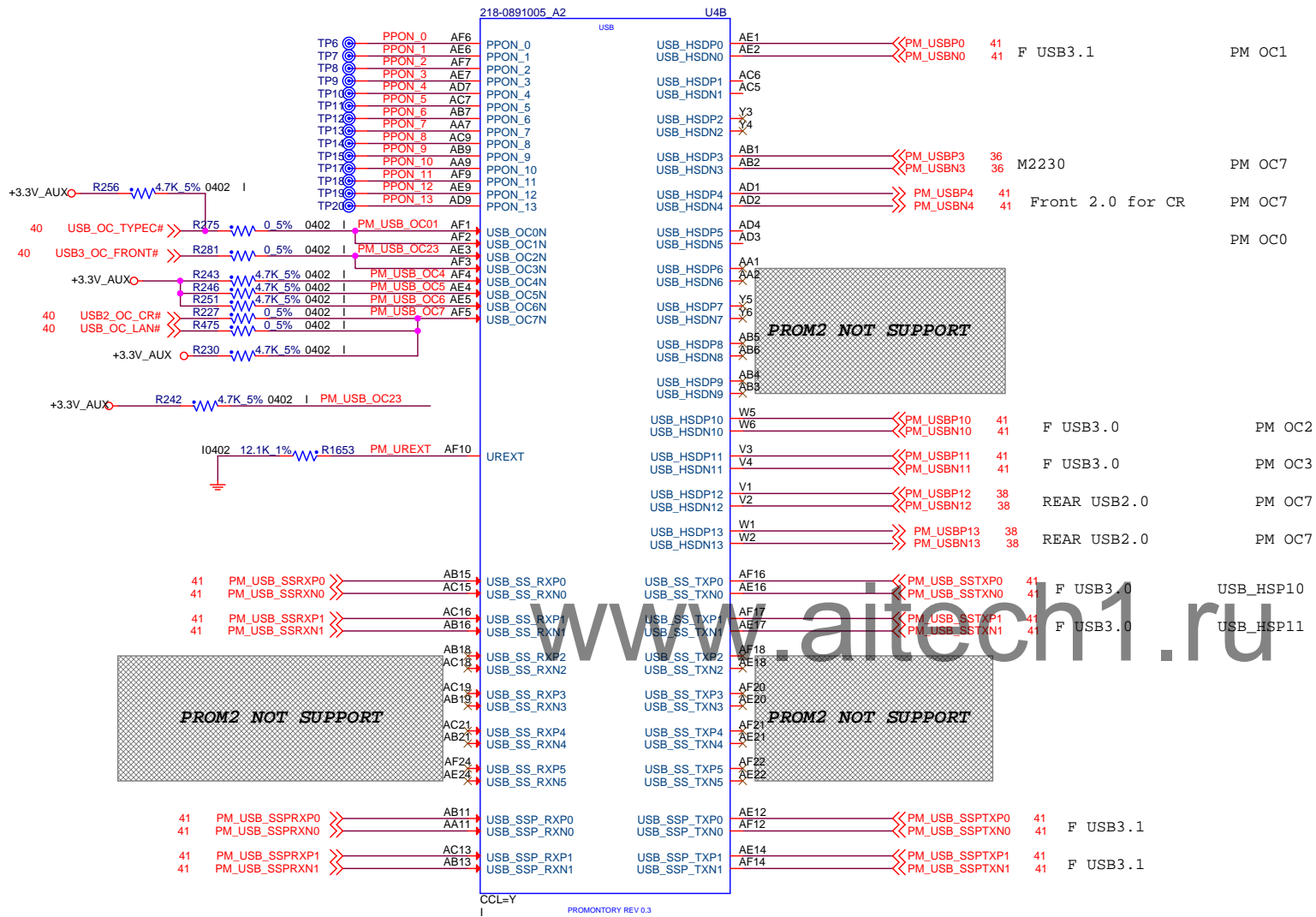


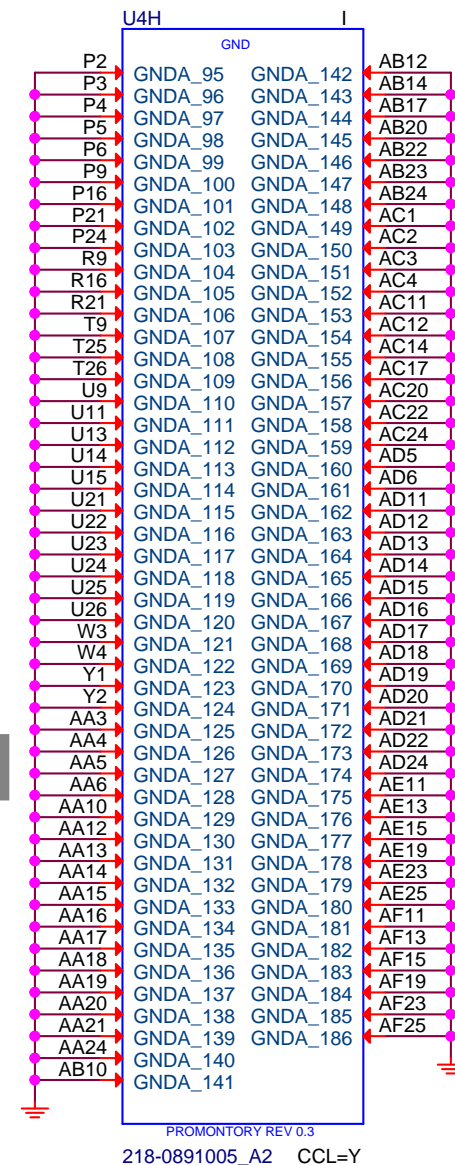
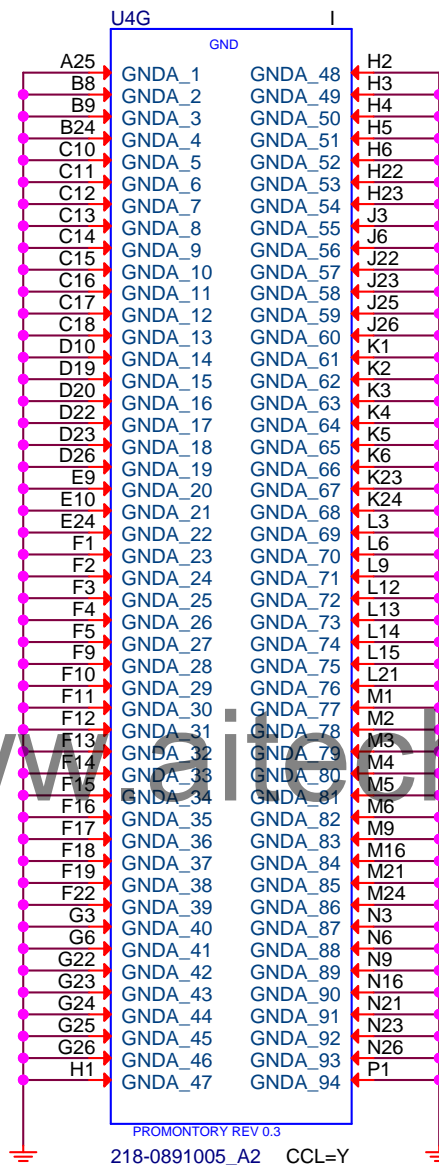
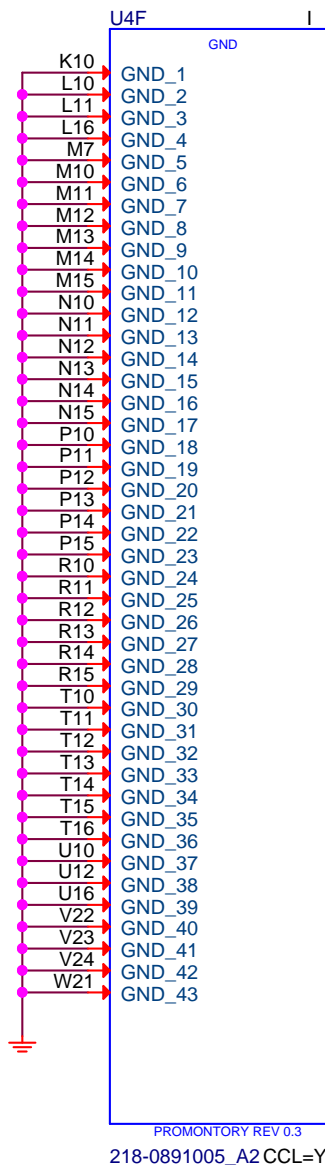
www.aitech1.ru

		HP RESTRICTED (HP RESTRICTED SECRET)	
		THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
DRAWN BY Foxconn CMMSG DWHD			
Title DDR3 CHB DIMM0			
Size	Document Number	Rev	
Custom	921822-000	X2	
Date: Tuesday, June 20, 2017		Sheet	19 of 68

Socket Color : BLACK







HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY **FOXCONN**

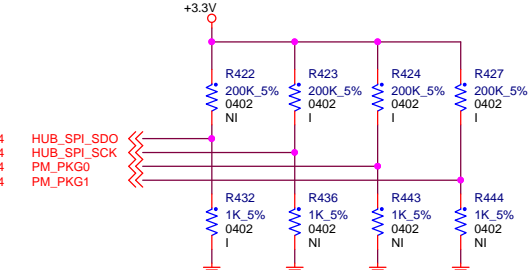
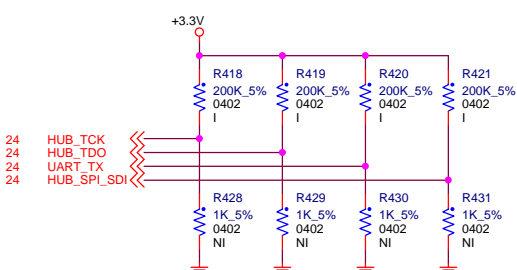
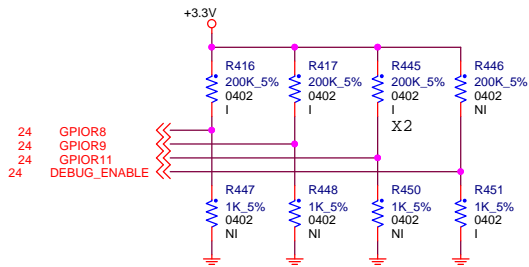
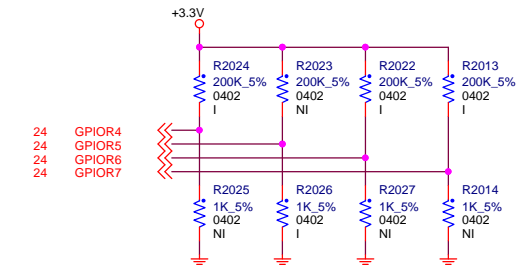
Title
FCH - GND/ PLL

Size A Document Number
921822-000

Rev
X2

Date: Tuesday, June 20, 2017

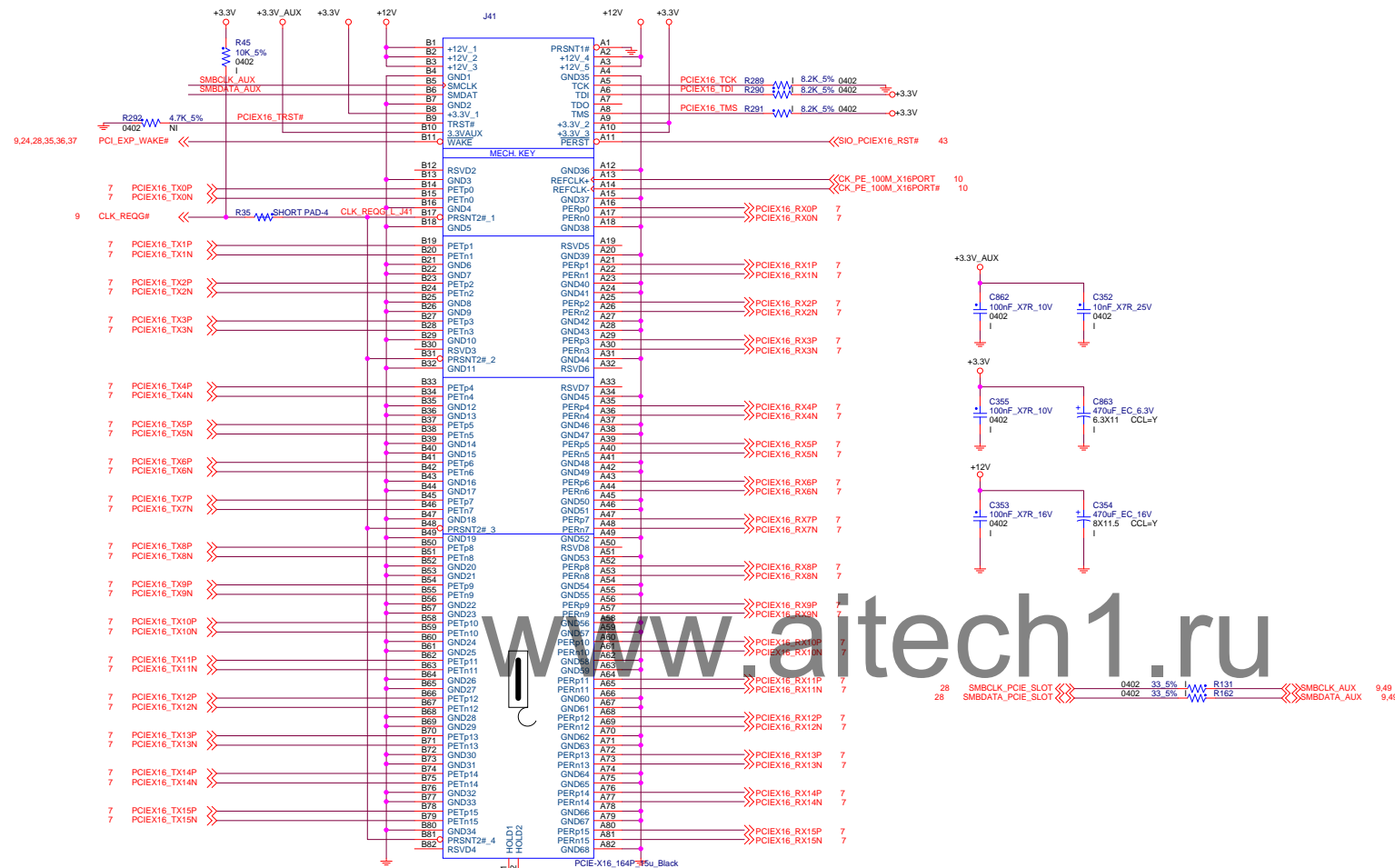
Sheet 25 of 68



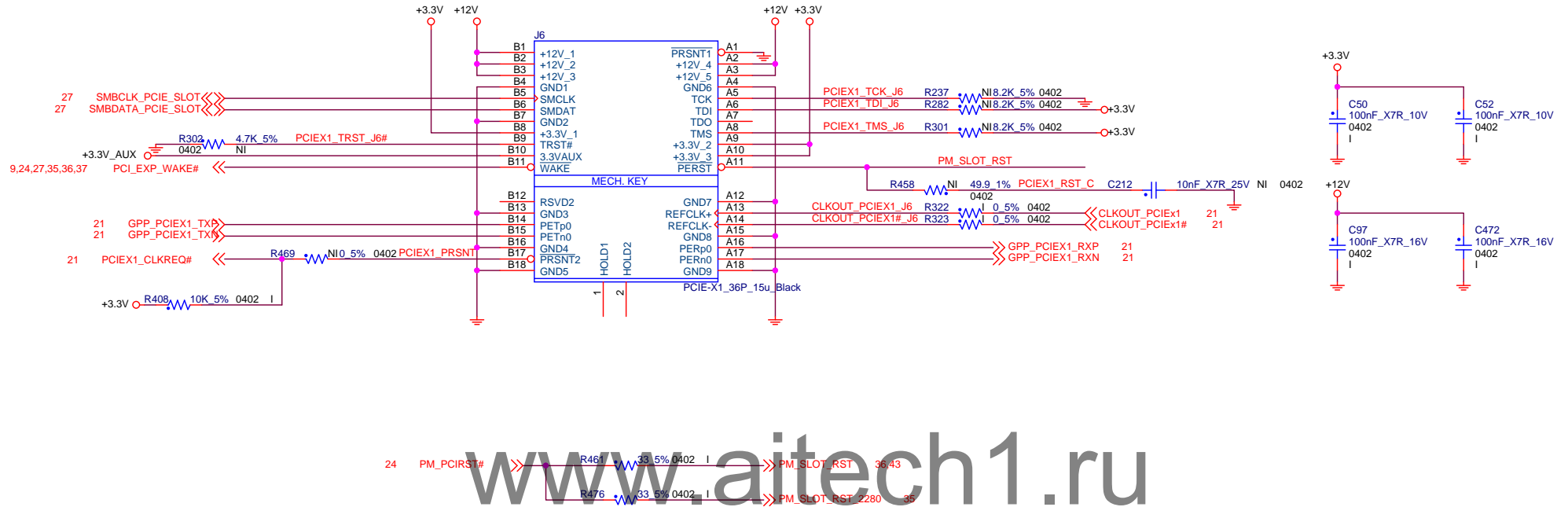
Strapping Pins	Function
TESTEN	Test mode enable 1: Test mode 0: Function mode
IFDET1	SATA Express port1 1: PCIe mode 0: SATA mode
IFDET0	SATA Express port0 1: PCIe mode 0: SATA mode
DEBUG_ENABLE	1:Debug mode 0:Function mode
TCK(DEBUG_SEL1)	11: Debug signal group 3 output 10: Debug signal group 2 output 01: Debug signal group 1 output 00: Debug signal group 0 output
TDO(DEBUG_SEL0)	
UART_TX(GPP_G1_SET1)	GPP Group1 11: 1 PCIe x4 10: 1 PCIe x2+2 PCIe x1
SPI_SDI(GPP_G1_SET0)	01: 4 PCIe x1 00: Reserved
SPI_SDO(GPP_G0_SET1)	GPP Group0 11: 1 PCIe x4 10: 1 PCIe x2+2 PCIe x1 01: 4 PCIe x1 00: Reserved
SPI_SCK(GPP_G0_SET0)	
GPIO_R4	1:GPP clock source from APU_CLKP/N 0:GPP clock source from Crystal also enable GPIO_R8
GPIO_R5	1:USB SSC disable 0:USB SSC enable
GPIO_R6	1:SATA SSC disable 0:SATA SSC enable
GPIO_R7	1:SATA Express SSC disable 0:SATA Express SSC enable
GPIO_R8 (enable from GPIO_R4)	1:GPP SSC disable 0:GPP SSC enable
GPIO_R11	1:GPP clock output enabled 0:GPP clock output disable


www.aitech1.ru

PCI EXPRESS x16 SLOT

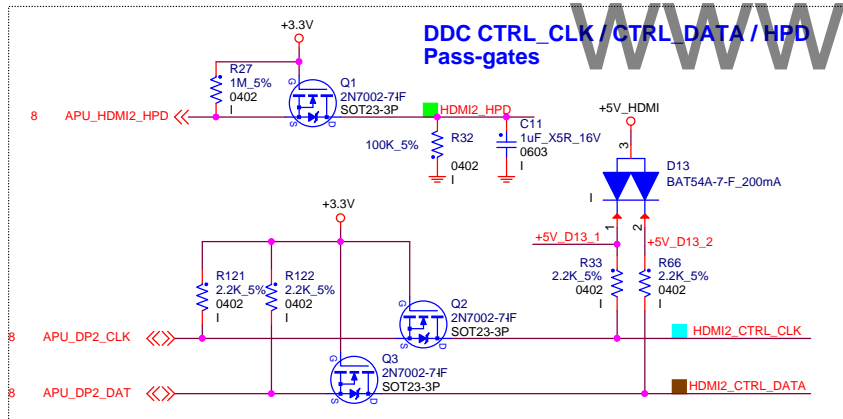
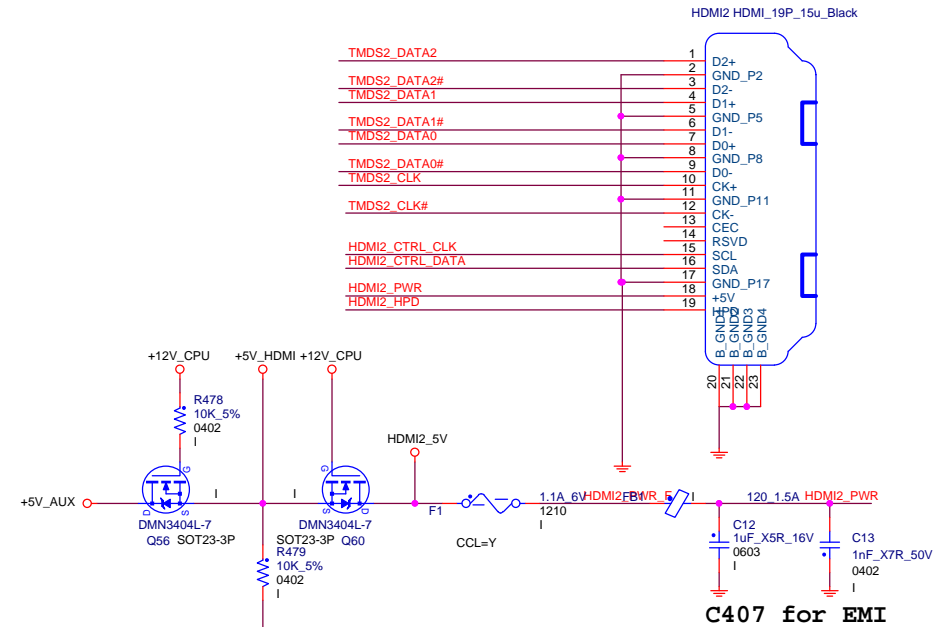
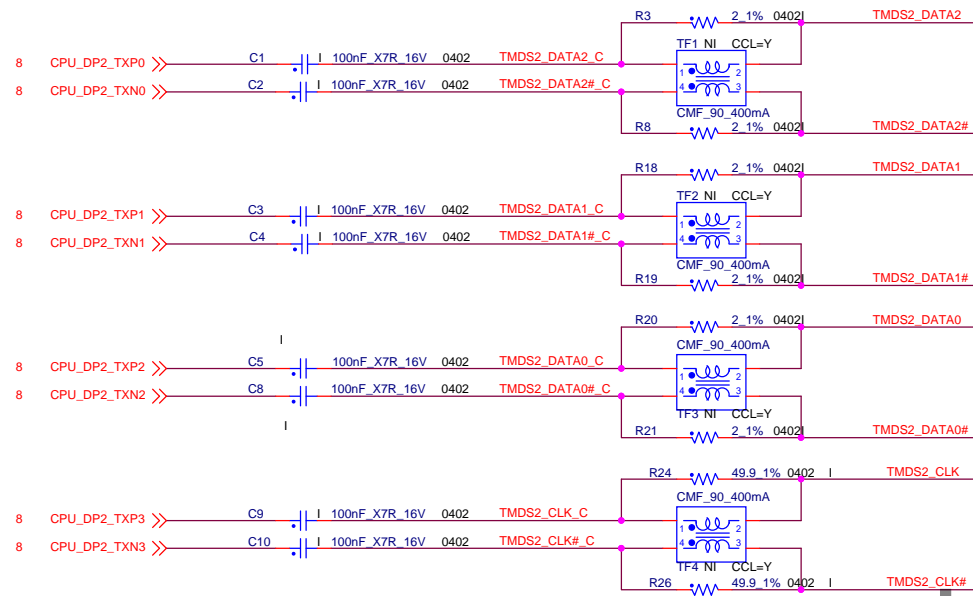


PCI EXPRESS X1 SLOT1

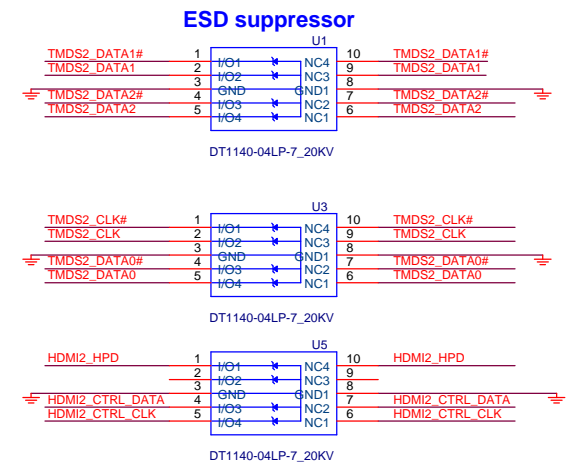
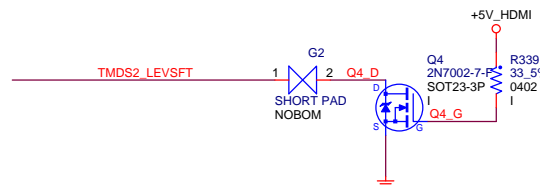
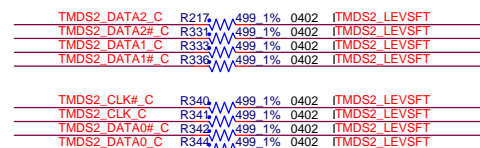


 HP RESTRICTED (HP RESTRICTED SECRET) THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
DRAWN BY FOXCONN	
Title PCIE x1 Connector	
Size B	Document Number 921822-000
Date: Tuesday, June 20, 2017	Rev X2
Date: Tuesday, June 20, 2017 Sheet 28 of 68	

HDMI 2



Cost Reduced Level Shifter Solution



HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY **FOXCONN**

Title **Display Port 1**

Size Document Number

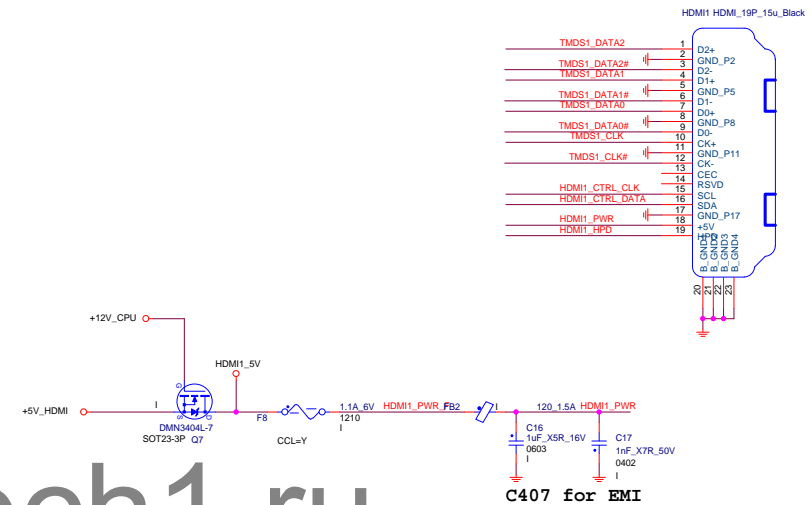
Custom 921822-000

Date: Tuesday, June 20, 2017

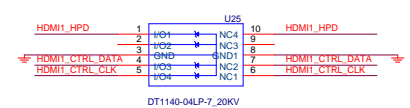
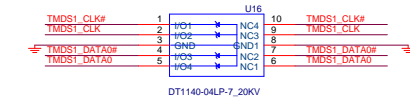
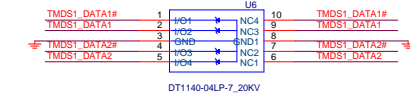
Rev **X2**

Sheet 29 of 68

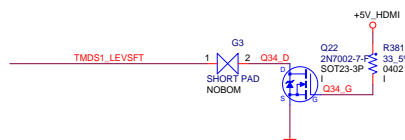
Total=136.8uW=0.14mW

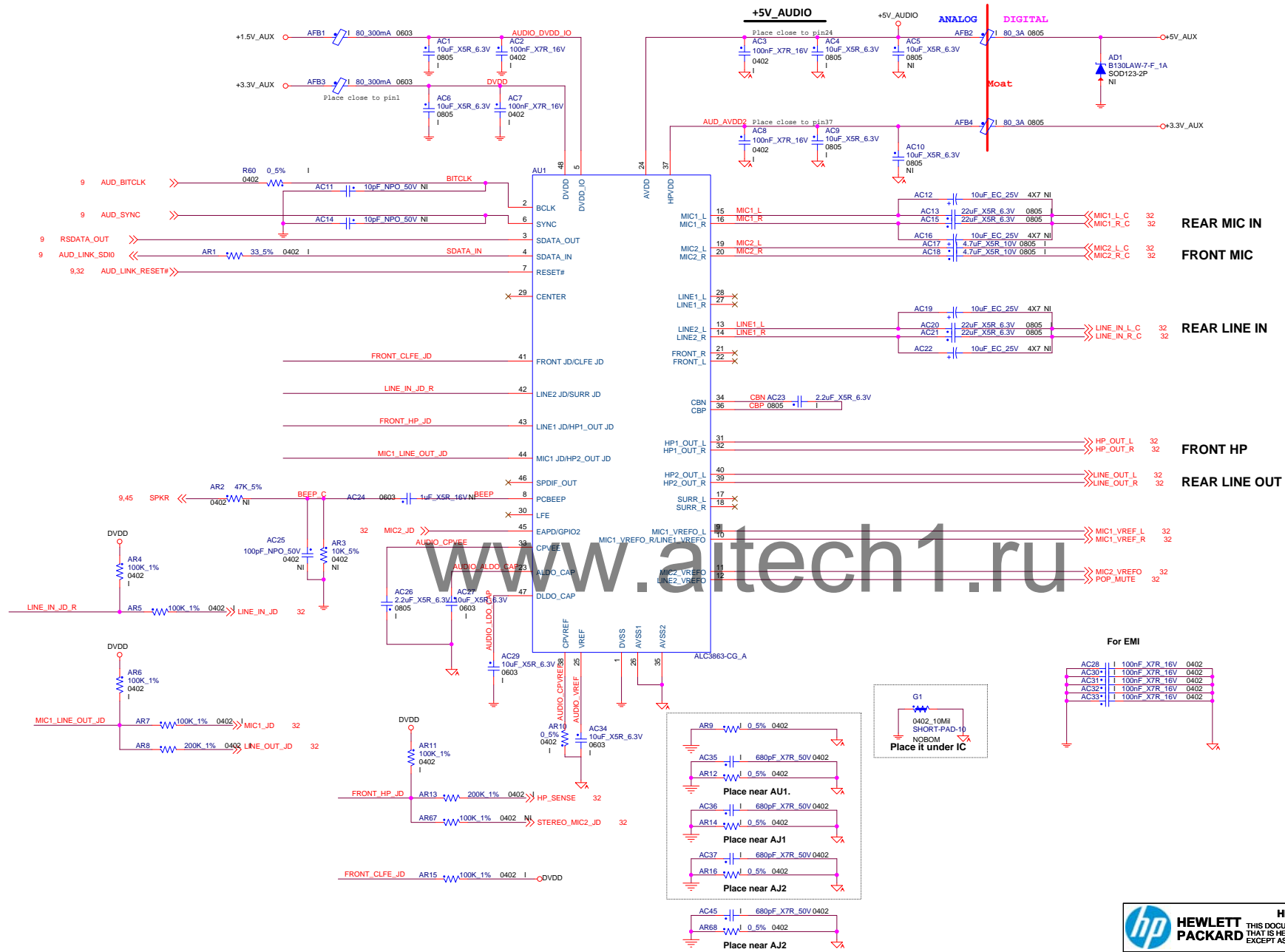


ESD suppressor

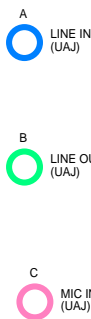
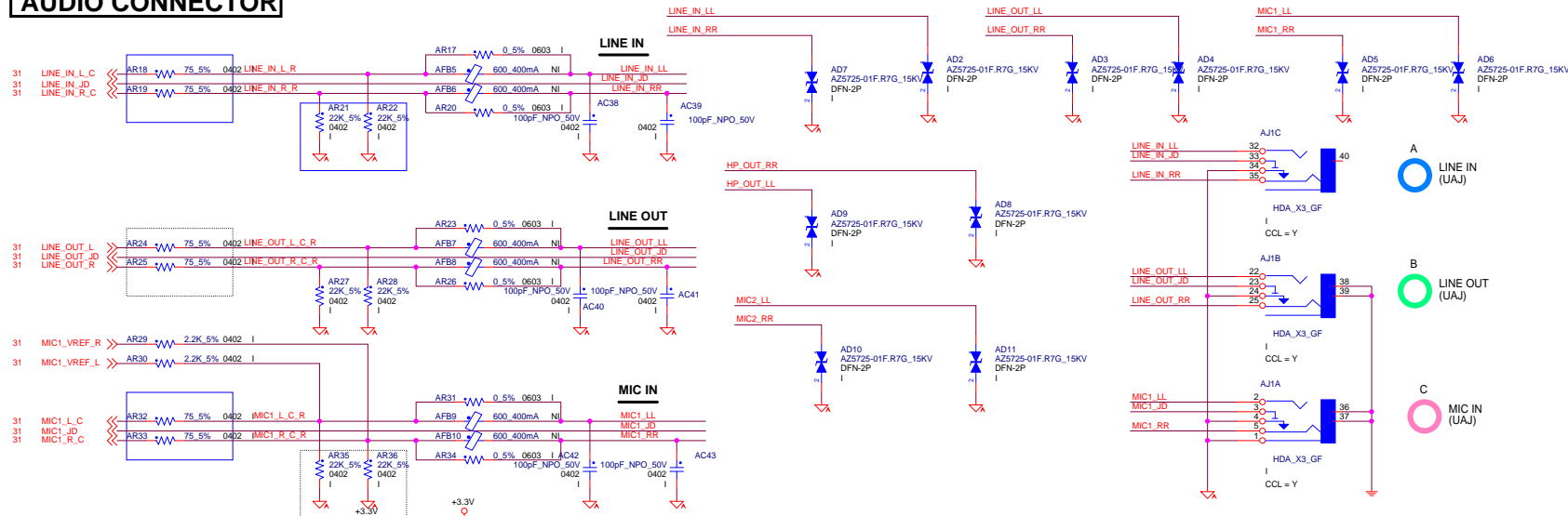


Co-layout with U6



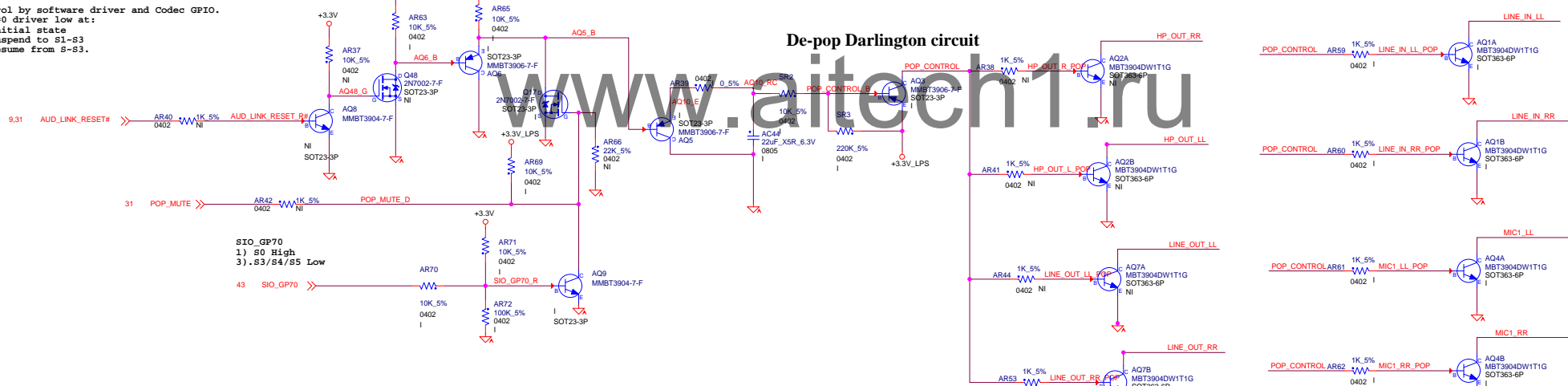


AUDIO CONNECTOR

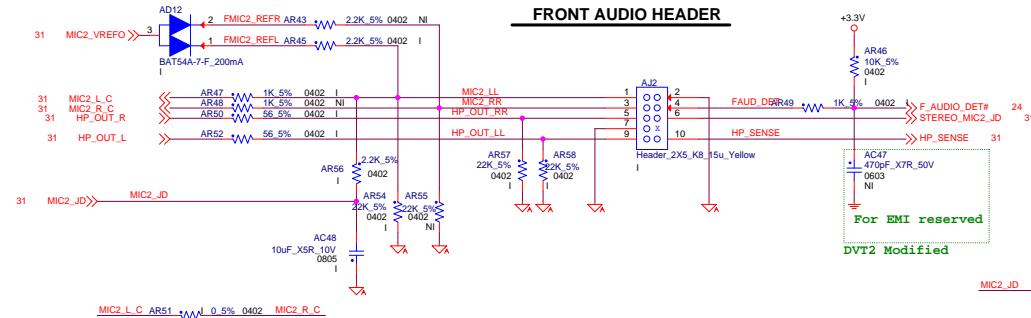


Control by software driver and Codec GPIO.
GPIO#0 driver low at:
1). Initial state
2). Suspend to S1-S3
3). Resume from S-S3.

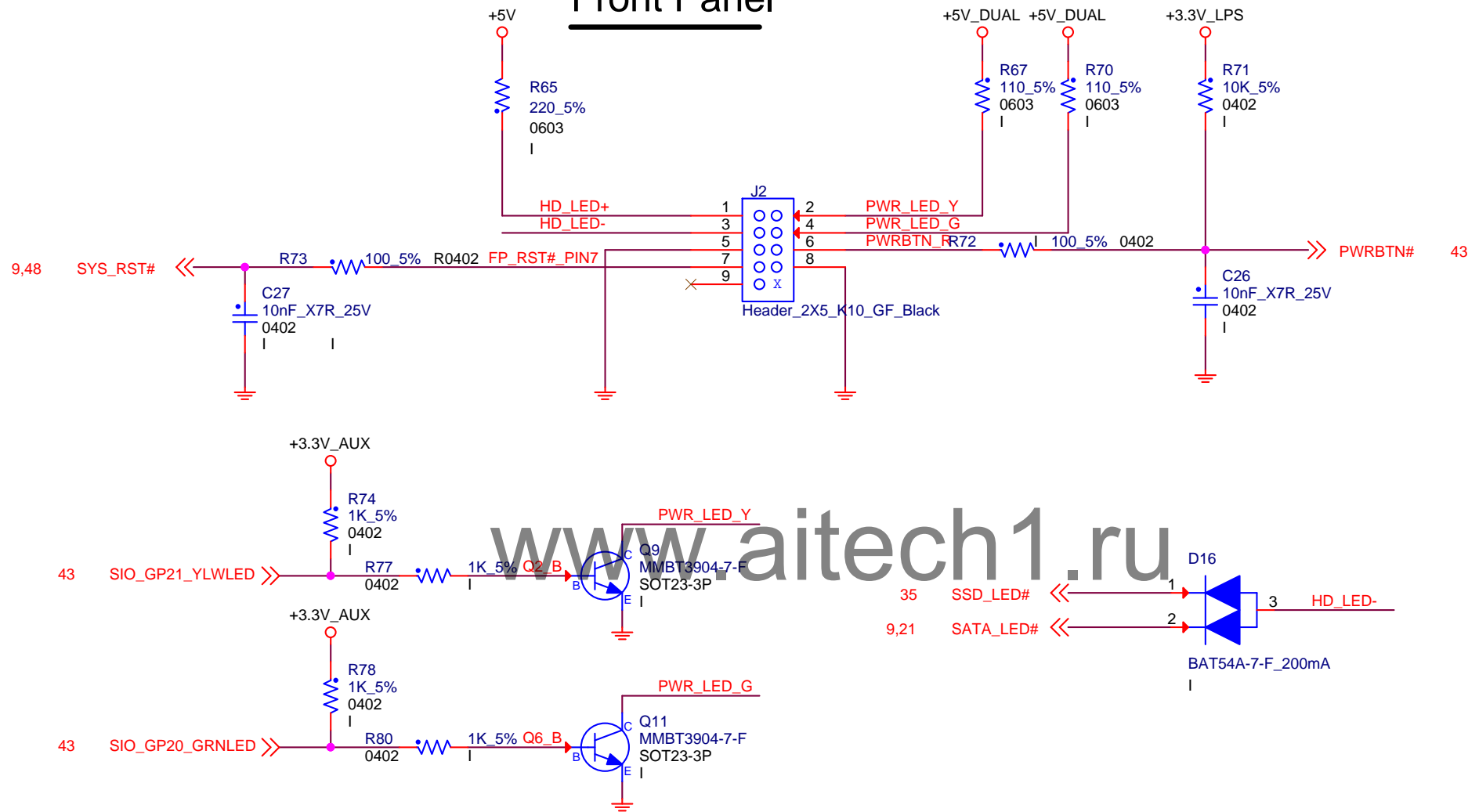
De-pop Darlington circuit



FRONT AUDIO HEADER



Front Panel



**HEWLETT
PACKARD**

HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP). DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY **FOXCONN**

Title
FRONT PANEL

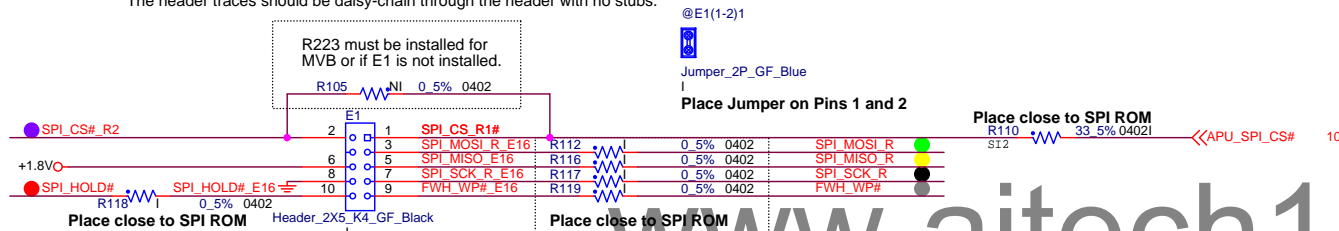
Size
A Document Number
921822-000

Rev
X2

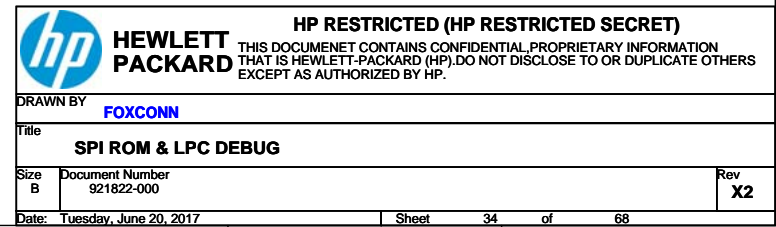
Date: Tuesday, June 20, 2017

Sheet 33 of 68

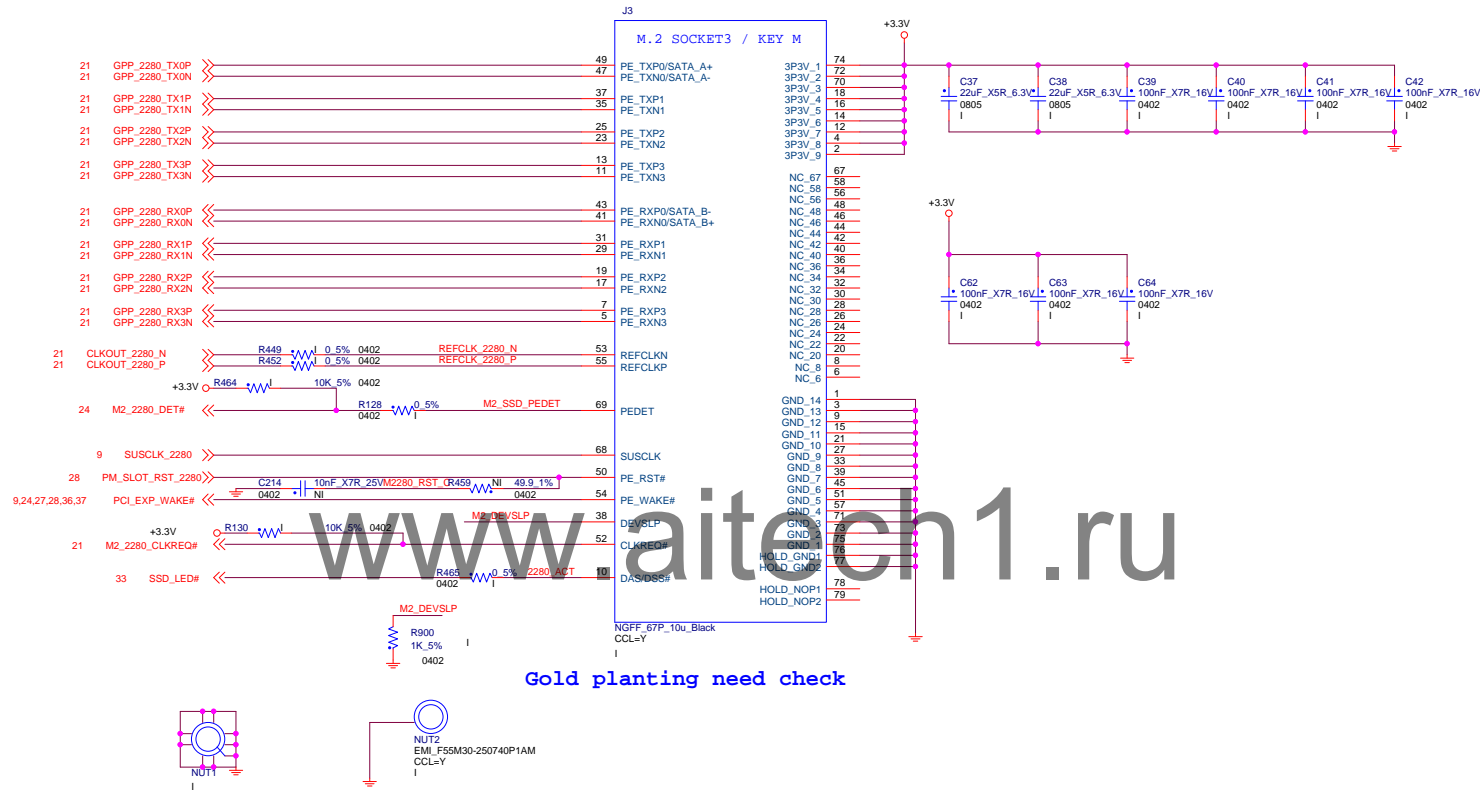
The header traces should be daisy-chain through the header with no stubs.



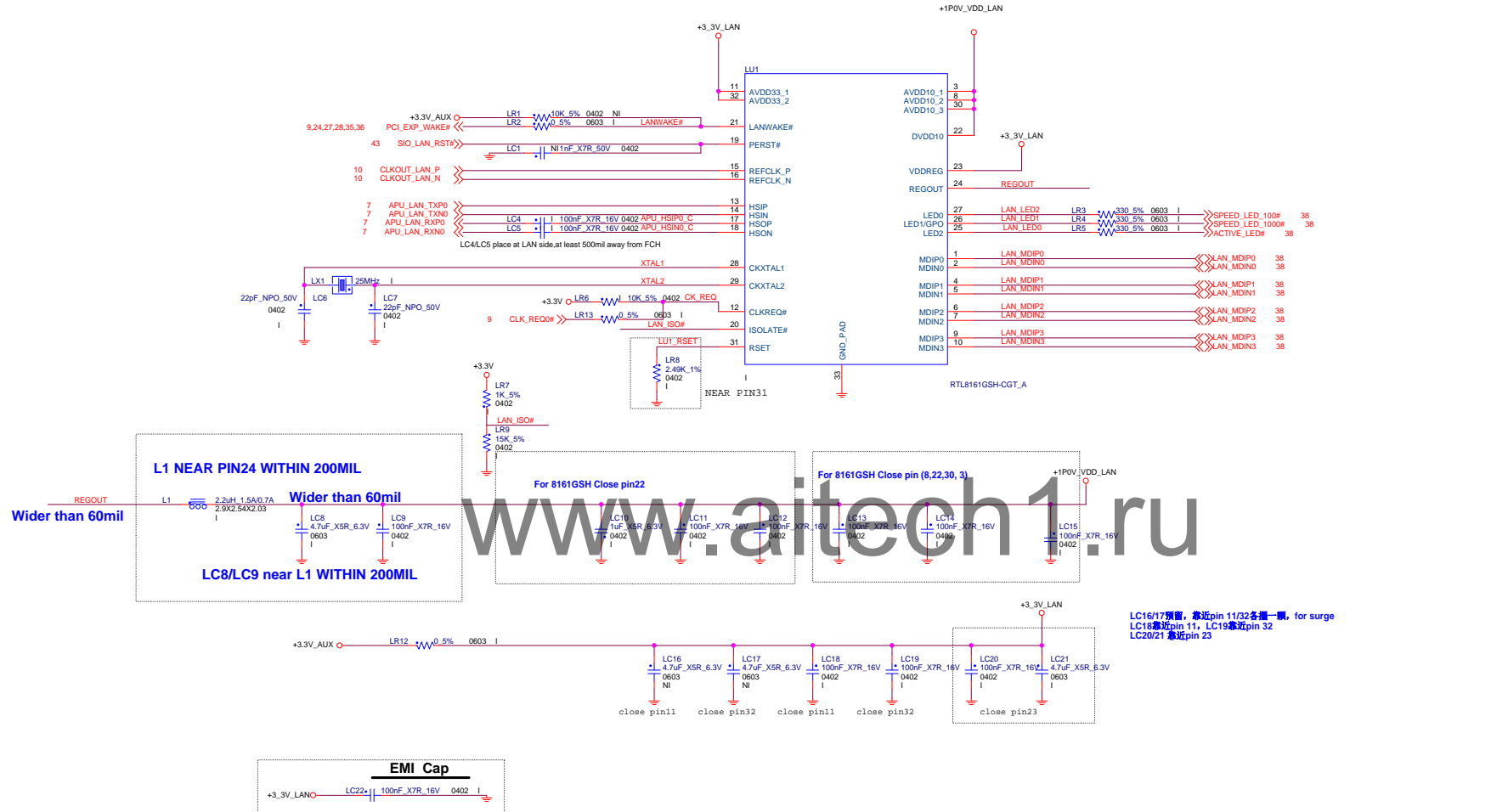
Timing diagram for the LPC1114 showing signals connected to the F2 header. The diagram includes signals like LPC_FRAME#, LPC_AD3_DBG, LPC_AD0_DBG, LPC_RST#, and APU_PCIE_RST# on the left, and SER_IRQ, LPC_AD1, LPC_AD2, CLK_LPC_33MHz, and Header_2X6_K7_GF_Black on the right. Each signal line is annotated with its pin number, a resistor value (R123, R125, R127, R159, R160), a delay (0.5%), a width (0402), and a polarity (I or NI).



M2. 2280 - STORAGE

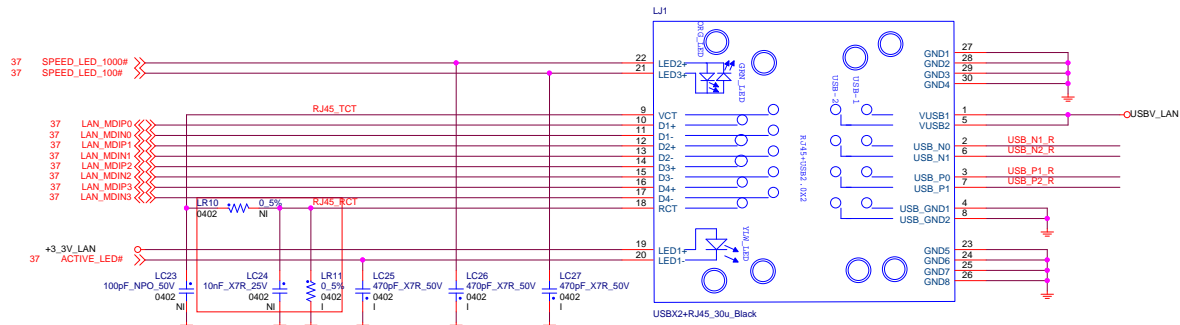


Realtek RTL8161GSH-CGT



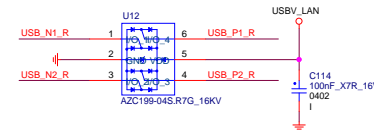
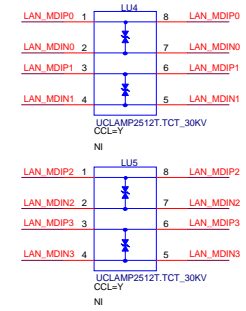
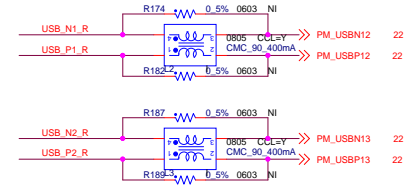
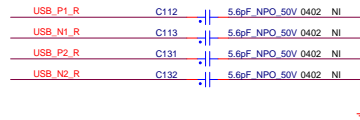
LC16/17 100nF, 16V, 0402, for surge
LC18 100nF, 16V, 0402, for surge
LC19 100nF, 16V, 0402, for surge
LC20/21 100nF, 16V, 0402, for surge

EMI Cap



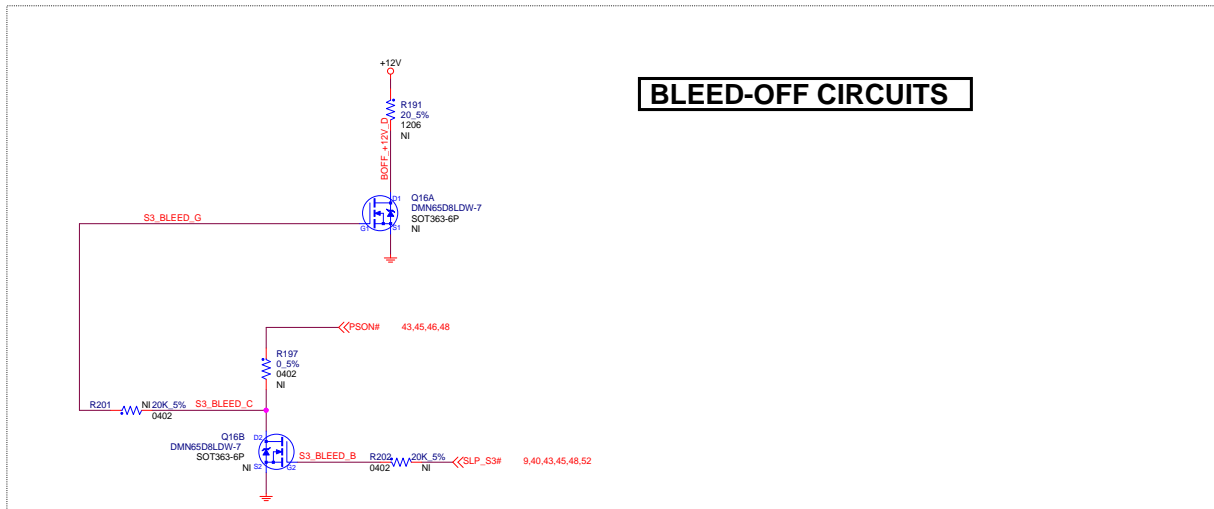
LR19 NI since pin18 has internally connect to GND

10/100M : LC30, LR18==> I, LR19 ==> NI
1000M : LC30, LR18 ==> NI, LR19 ==> I



www.aitech1.ru

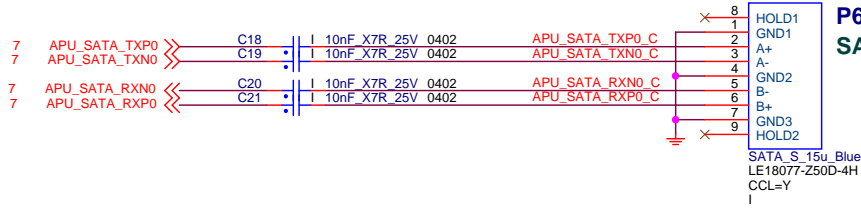
BLEED-OFF CIRCUITS



DARK BLUE (SATA 3.0)

**P6
SATA0**

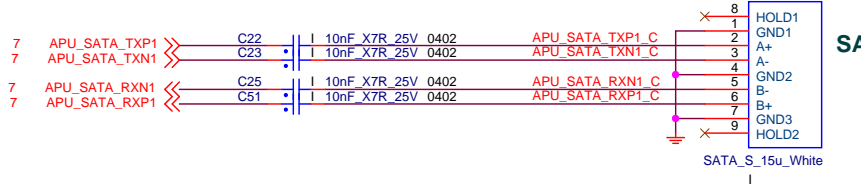
AM4 SATA0



WHITE (SATA 3.0)

SATA1

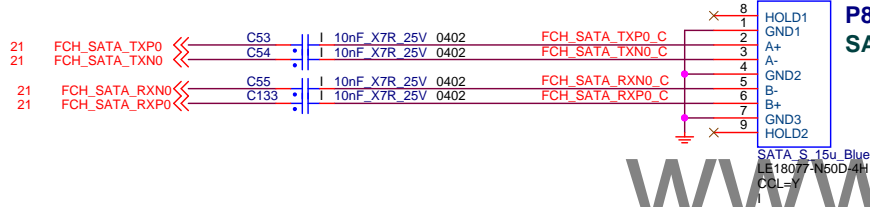
AM4 SATA1



LIGHT BLUE (SATA 3.0)

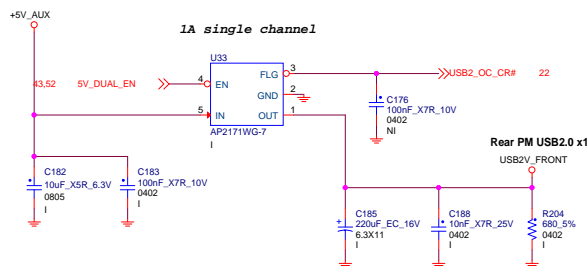
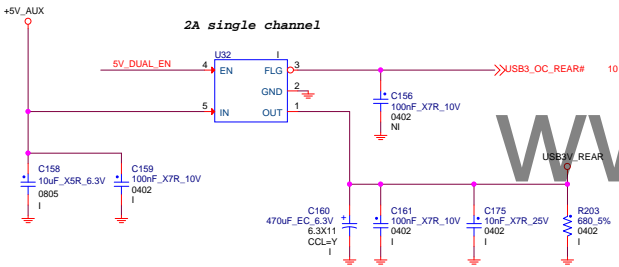
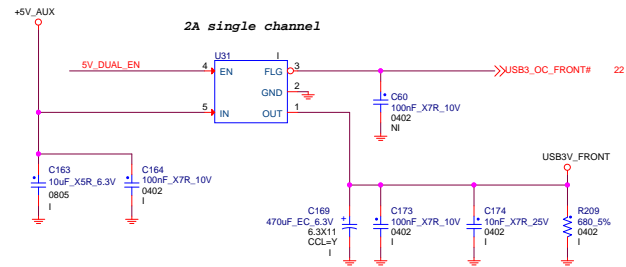
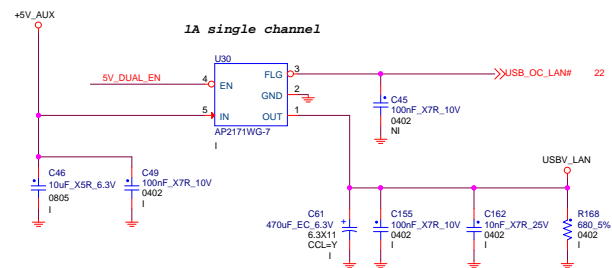
**P8
SATA2**

PM SATA2

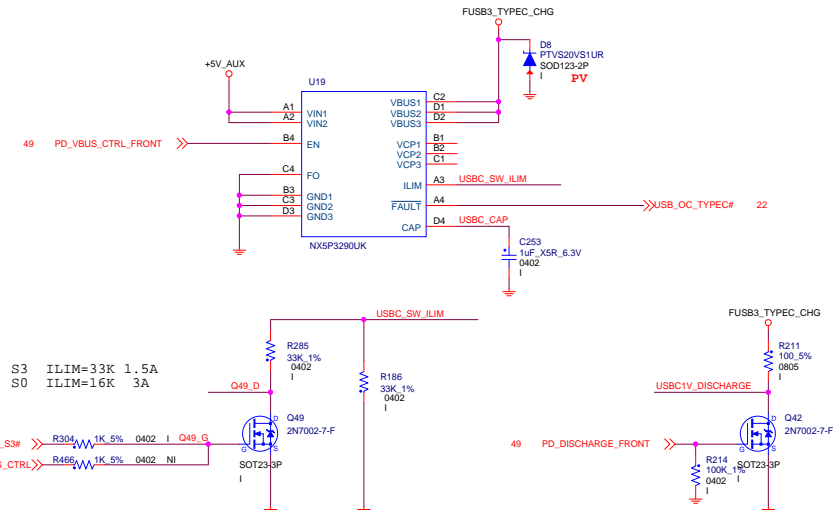


TX/RX connection need check

HEWLETT PACKARD		HP RESTRICTED (HP RESTRICTED SECRET)	
		<small>THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP).DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.</small>	
DRAWN BY FOXCONN			
Title SATA /PS2			
Size B	Document Number 921822-000		Rev X2
Date: Tuesday, June 20, 2017		Sheet 39 of 68	

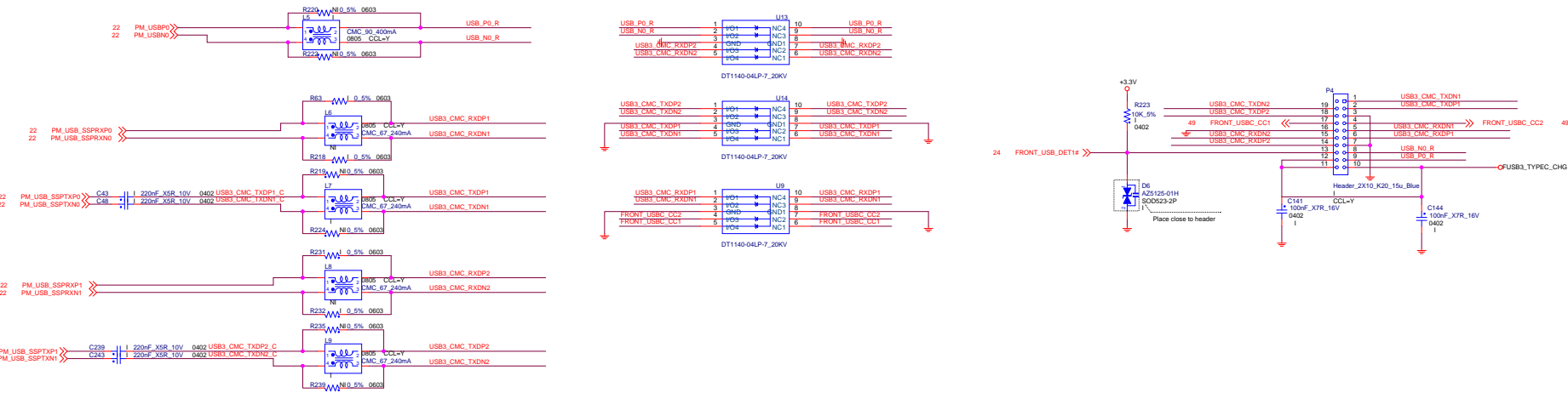


USB CHARGER

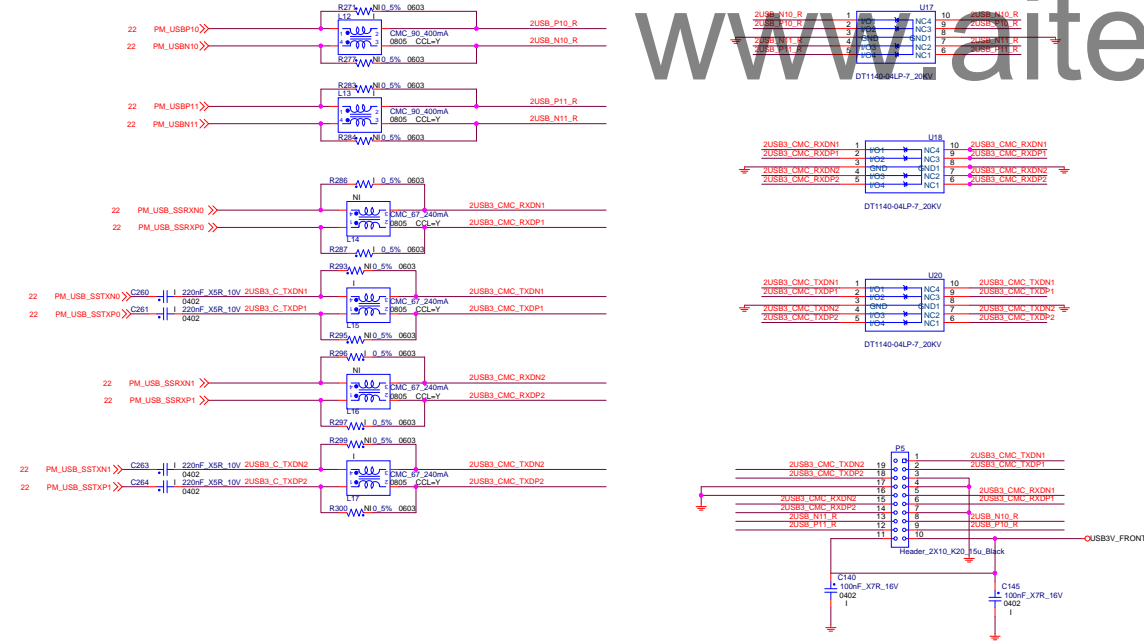


www.aitech1.ru

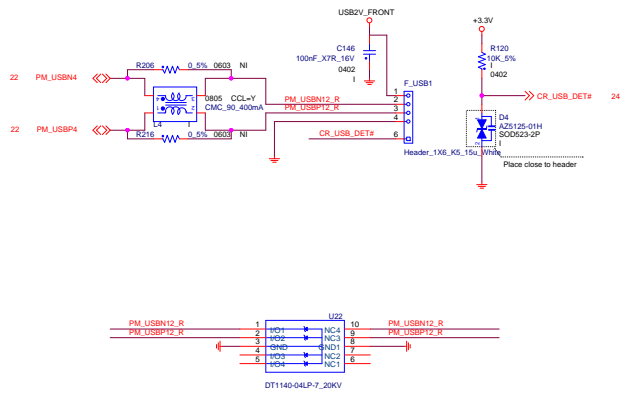
FRONT USB 3.1 typeC



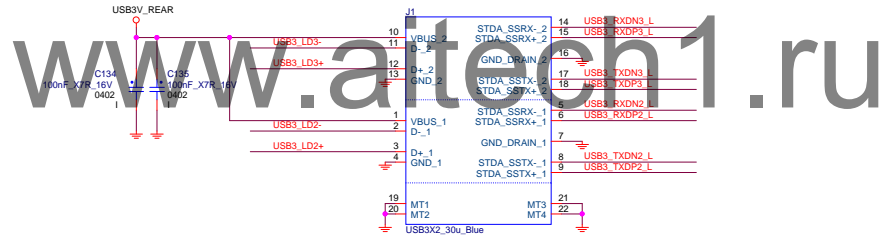
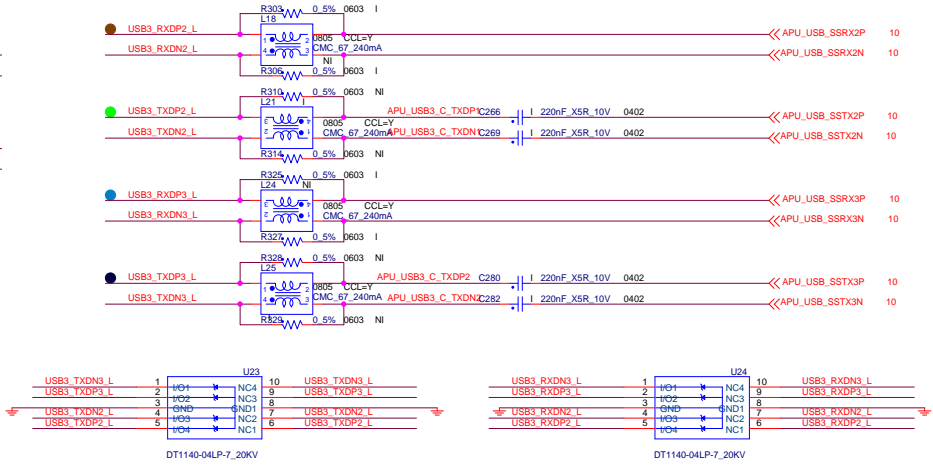
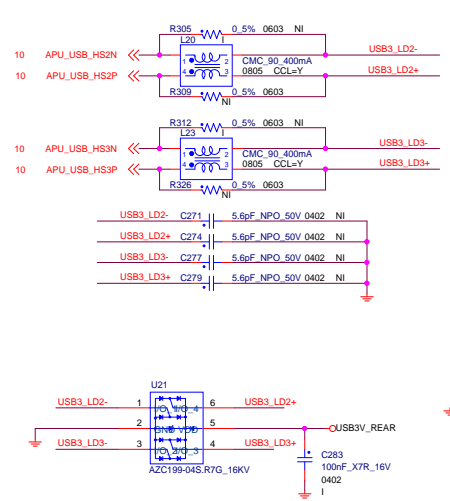
FRONT USB 3.0 x2



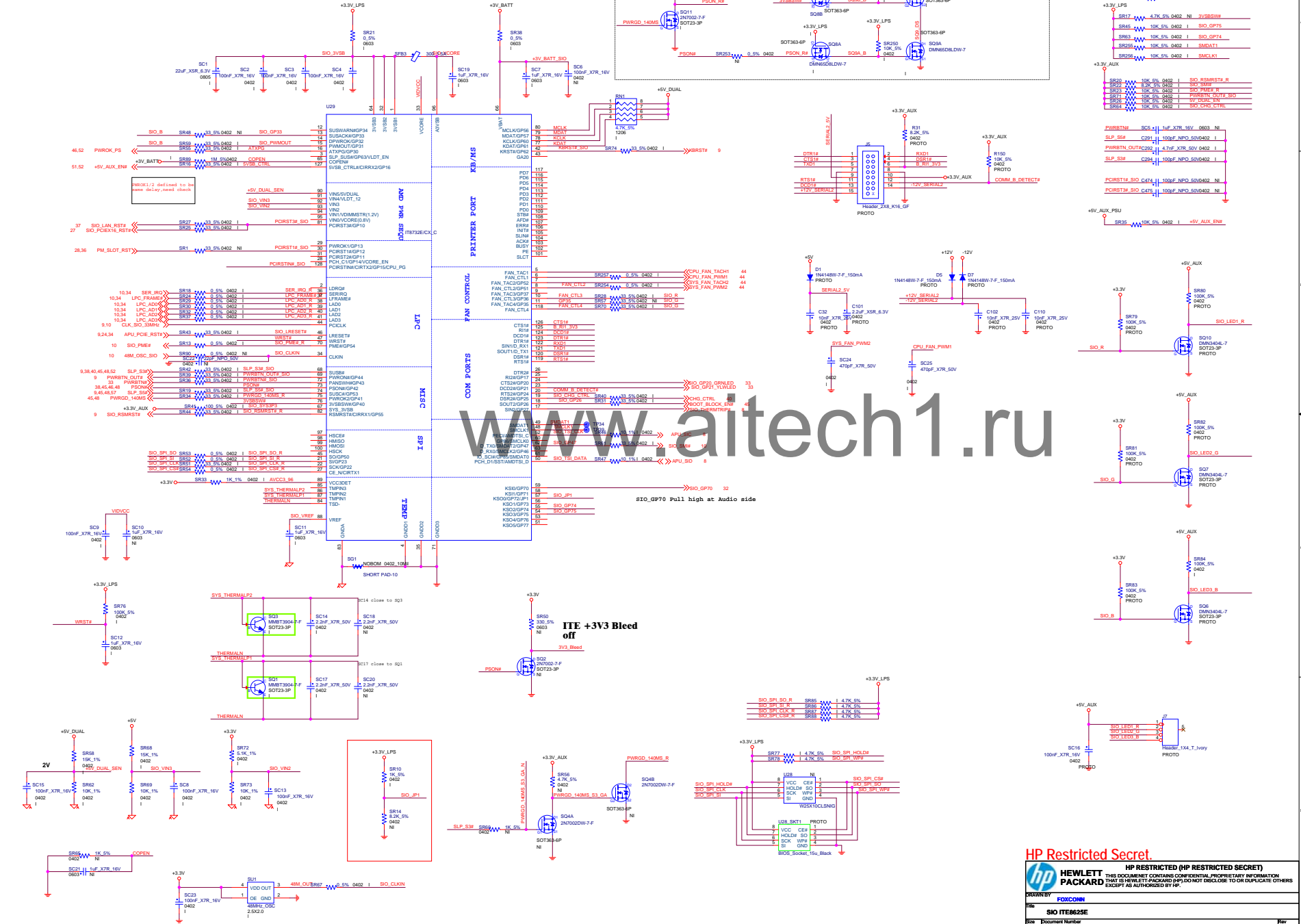
Front USB2.0 card reader



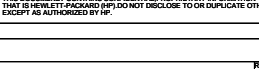
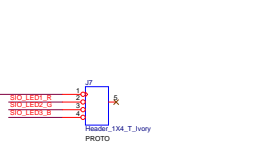
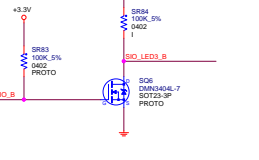
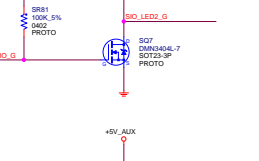
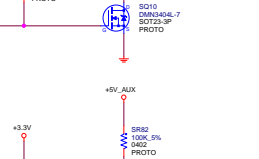
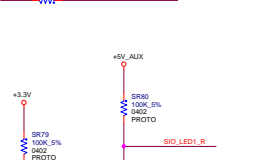
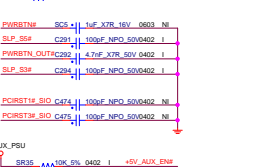
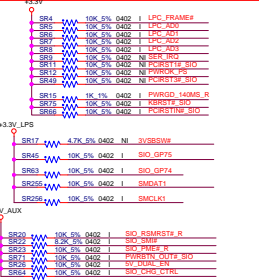
REAR USB



JP1	Symbol	Value	Description
Pin-45	DSW_EUP_SEL	1 RUP	
		0 DSW	

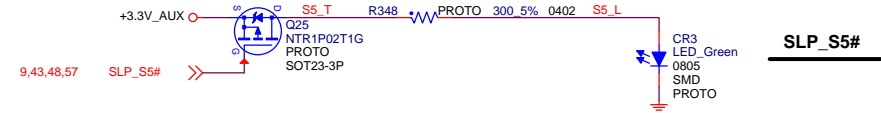
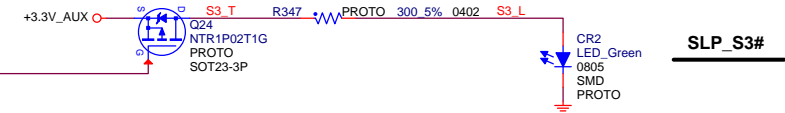


SR4 NI, LPC_FRAME has P270 pull high 10K
SR3 NI, P270 requires SR3_P270 pull up resistor

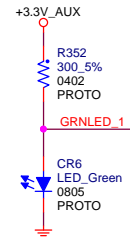


PCA LED

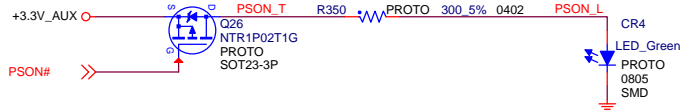
9,38,40,43,48,52 SLP_S3#



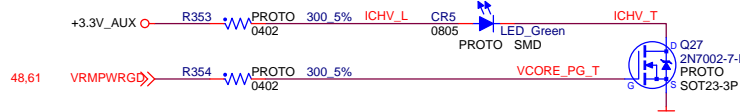
+3P3V_AUX



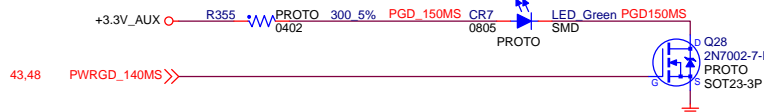
PSON#



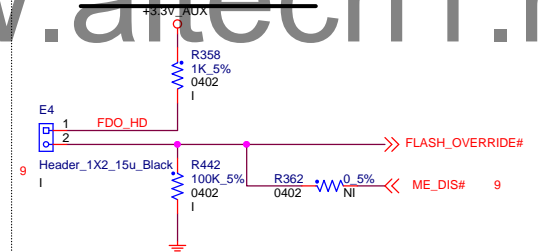
VRMPWRGD



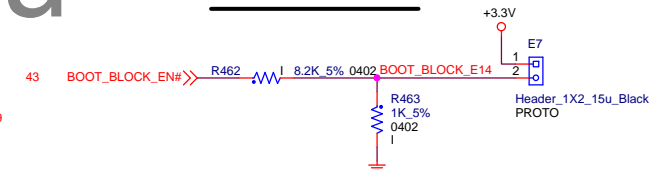
PWRGD_150MS



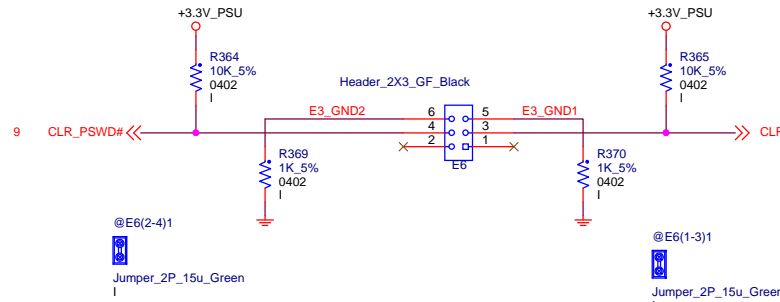
FLASH OVERRIDE(ME Disable)



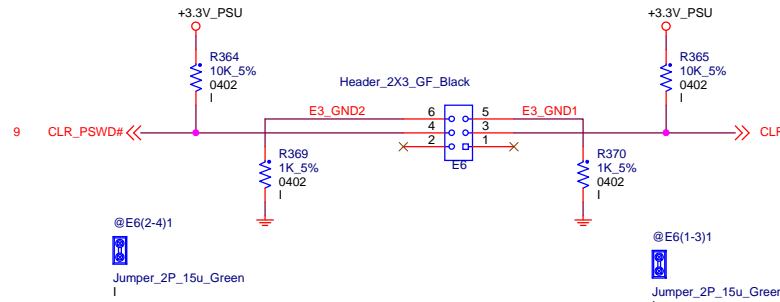
Boot block enable#



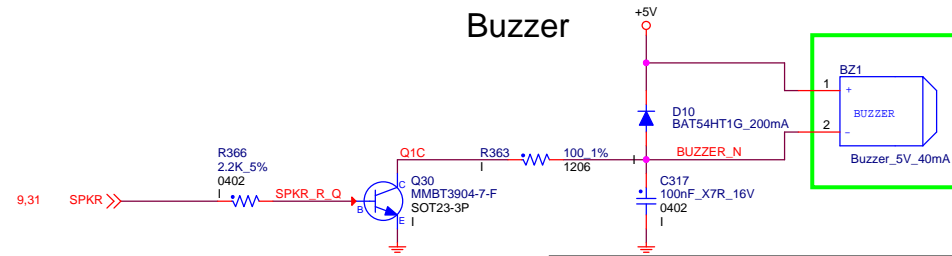
CLEAR PASSWORD



CLEAR CMOS



Buzzer



**HEWLETT
PACKARD**

HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP). DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY **FOXCONN**

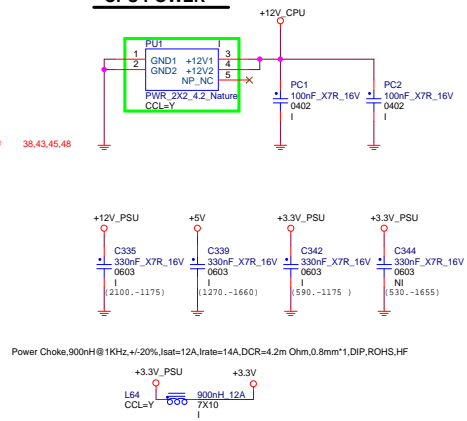
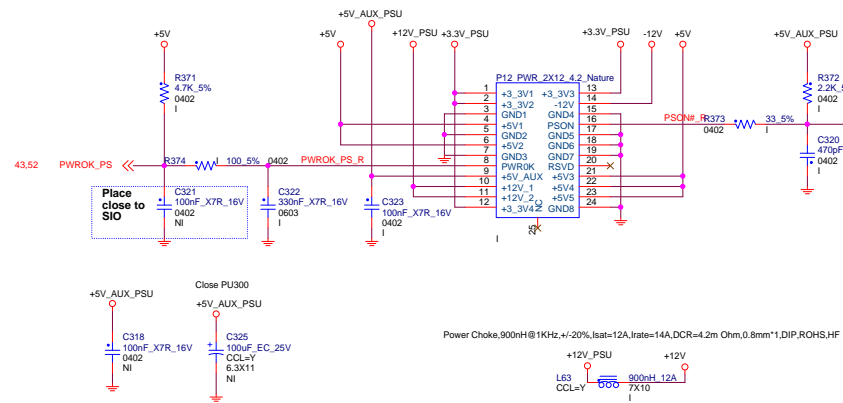
Title **LED / HEADER**

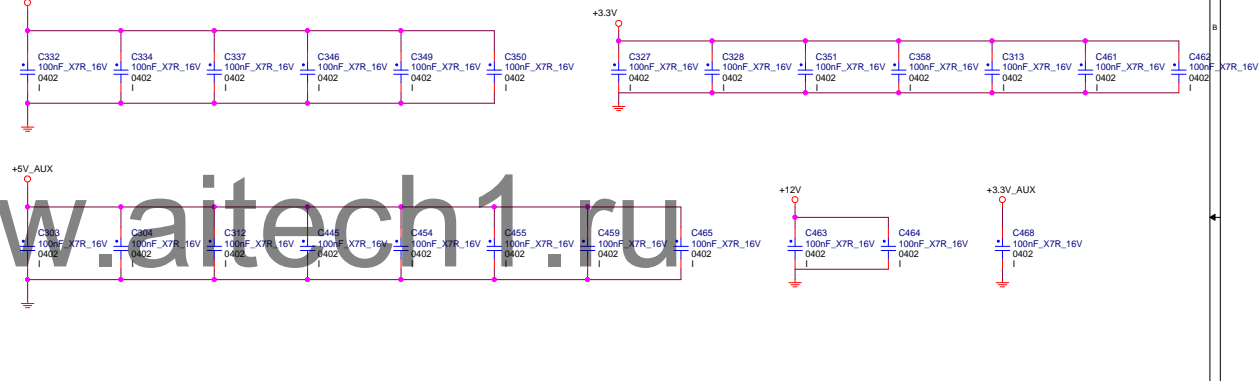
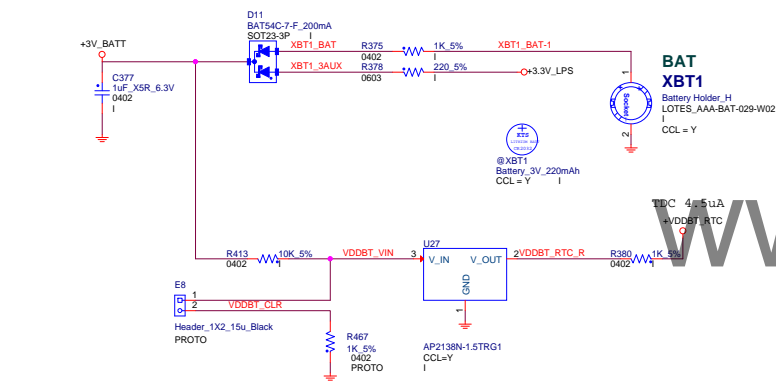
Size Document Number
Custom 921822-000

Date: Tuesday, June 20, 2017

Rev **X2**

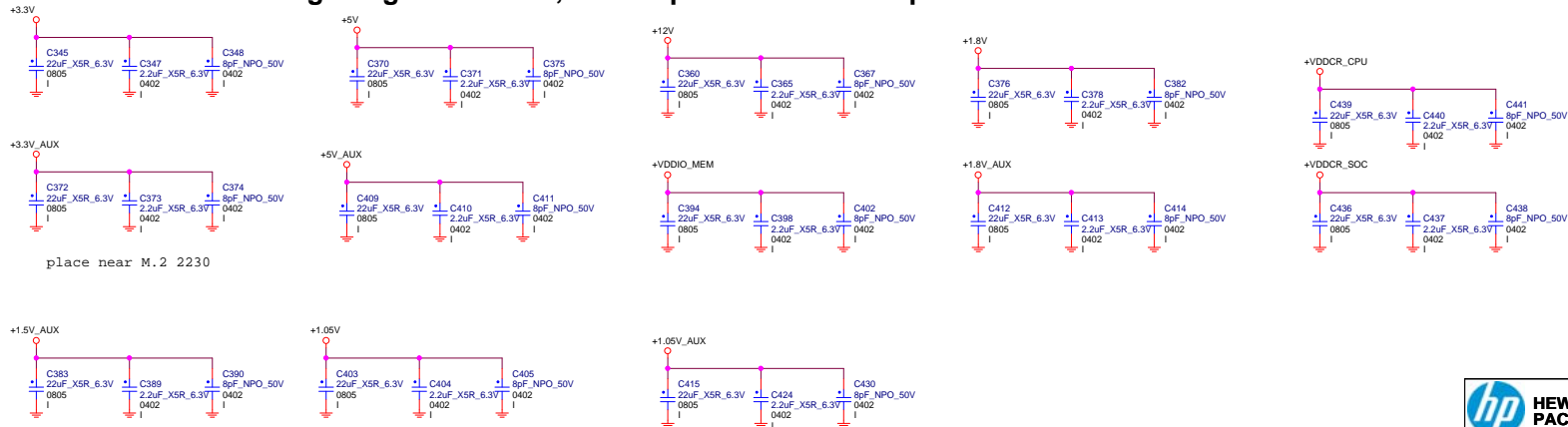
Sheet 45 of 68



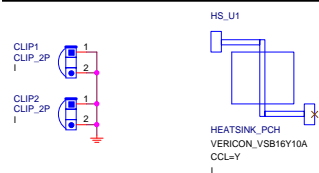
[illegible]

When +3V/+5V length bigger than 5cm, should place one team cap.

When +3V/+5V length bigger than 5cm, should place one team cap.



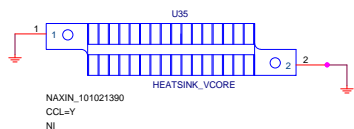
Promontory Heatsink



Bumper

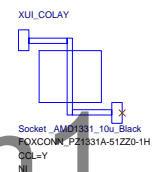
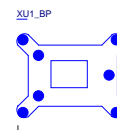
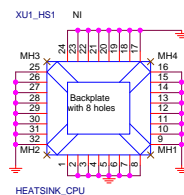


VCORE HEATSINK

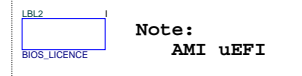


VGT HEATSINK

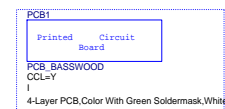
CPU HEATSINK



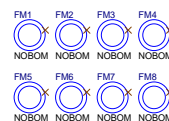
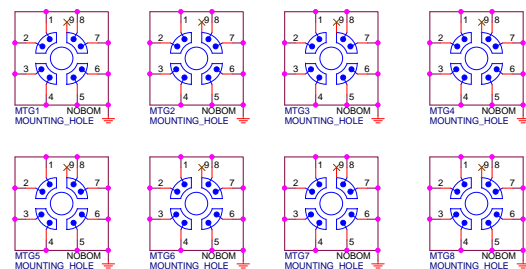
Licence Label



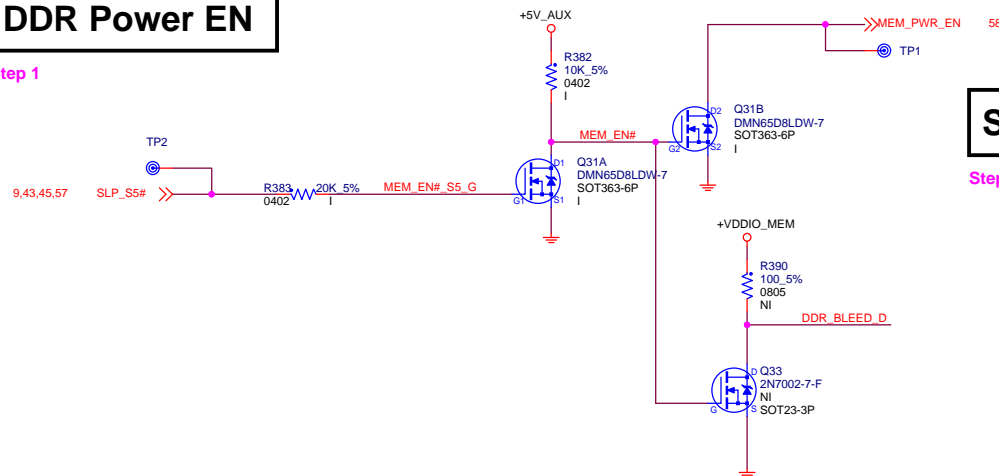
PCB



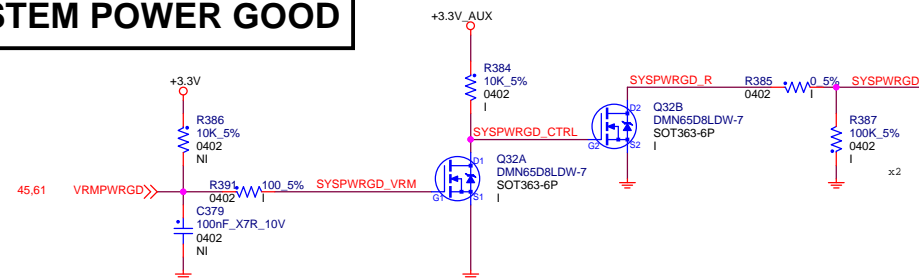
www.aitech1.ru



Step 1

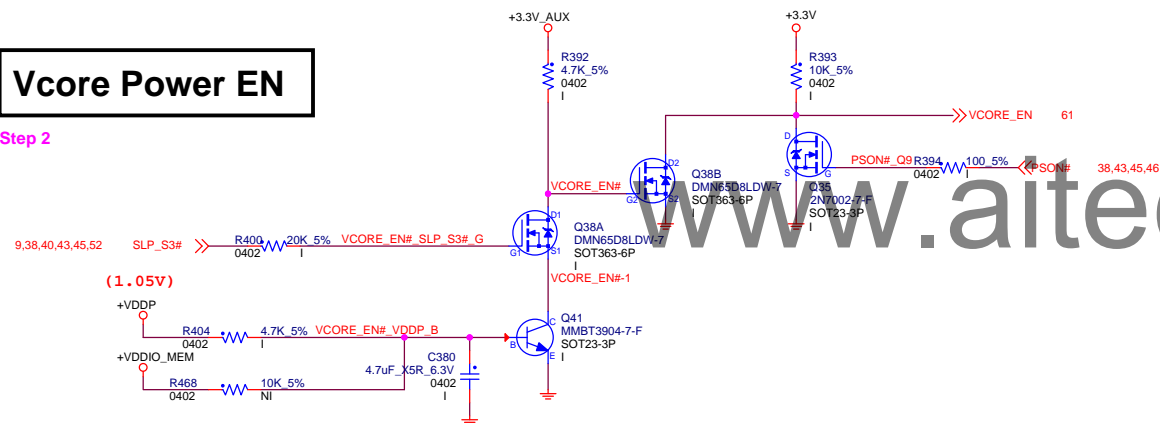


Step 3

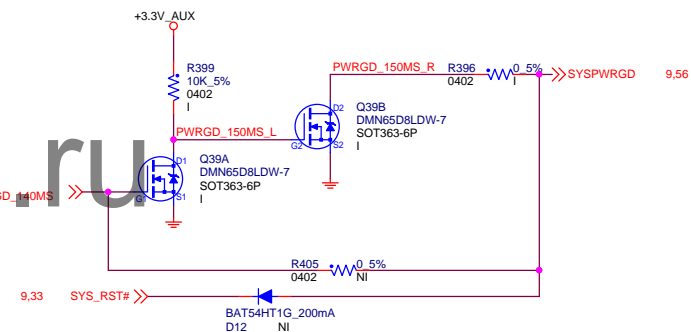


If use PWRGD1 connect to SYSPWRGD, need to use PWRGD1 connect to PWRGD_140ms.

Step 2



Step 4



HP RESTRICTED (HP RESTRICTED SECRET)

THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION
THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY

FOXCONN

Title

AMD Power Good Circuit

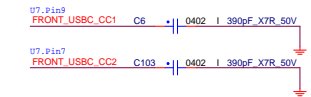
Size	Document Number
Custom	921822-000

Date: Tuesday, June 20, 2017

Rev	X2
-----	----

FRONT TYPEC PD Controller - DFP Only

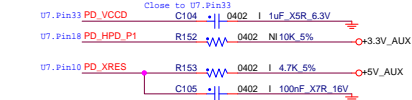
Leakage Voltage Protection for CC



SMBus/INT# Pull-Up

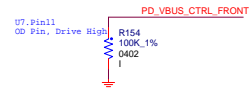
Already PU @ SIO Page26

PD Controller HW Setting

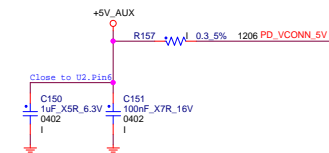


PD Controller HW Setting

Change List 1&2

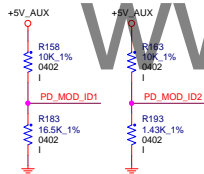


OCP Protection for VCONN

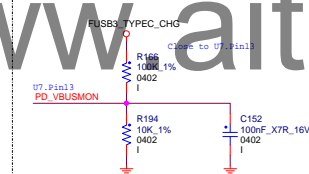


MOD_ID Selection

Note 1 Change List 3

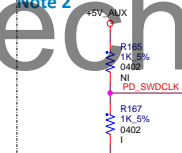


VBUS Monitor



SMBus Address Config.

Note 2

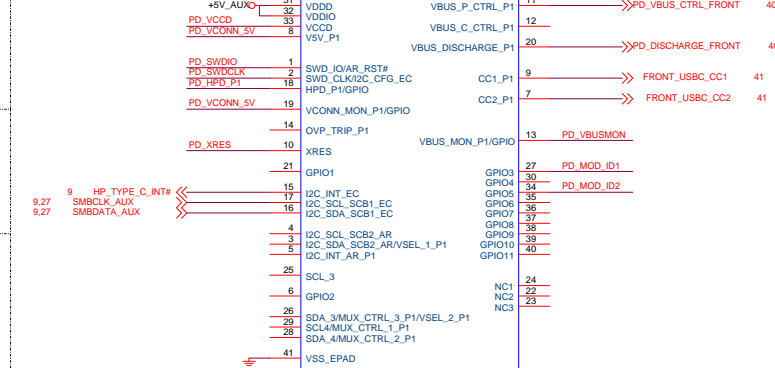


Change List

Following CCG4 Unified Schematics_HPv7_040816 to update.

1. Remove OVP Trip From CCG4 circuit. OVP can be floating.
2. VBUS CTRL directly connect to Power Switch.
3. Add MOD_ID selection for difference configuration mode. Please refer to Design Note1
4. Remove R104, U6, C58 for Item1&2 5. Add R369, R383, R370, R384 for Items3

Front TYPEC PD Controller



Design Note

Note 1

DFP Mode:
ID1 = L5 ; ID2 = L1
DFP+DP Mode
ID1 = L5 ; ID2 = L2

L0 = 0V
L1 = VDD/8
L2 = 2VDD/8
L3 = 3VDD/8
L4 = 4VDD/8
L5 = 5VDD/8
L6 = 6VDD/8
L7 = 7VDD/8

Note 2

SMBUS ADDRESS

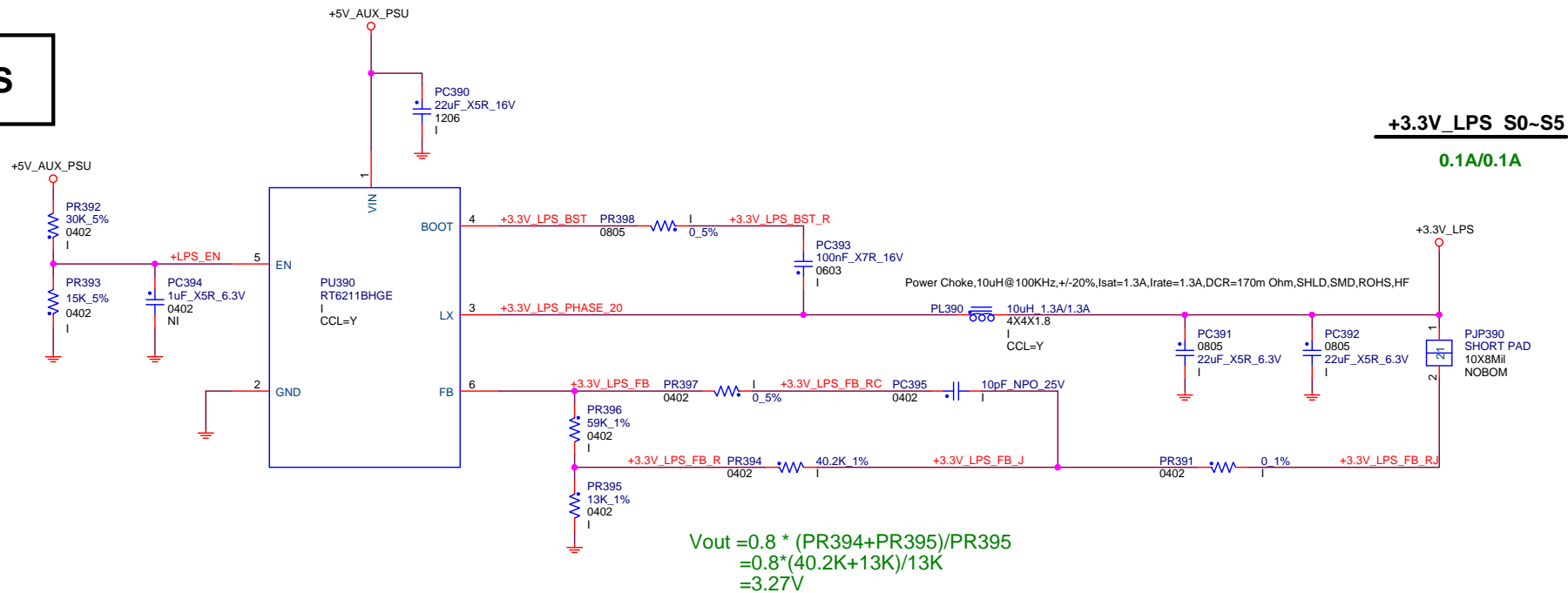
- 08 (when SWD CLK = floating)
- 40 (when SWD CLK = low)
- 42 (when SWD CLK = high)

The first will be 40 and the second will be 42.

if have 2 Type-C controllers:

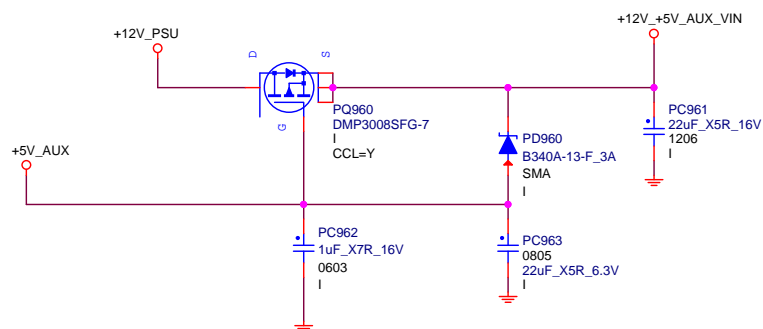
- 40 will be Dual Port controller.
- 42 will be Single Port controller.

+3.3V_LPS



www.aitech1.ru

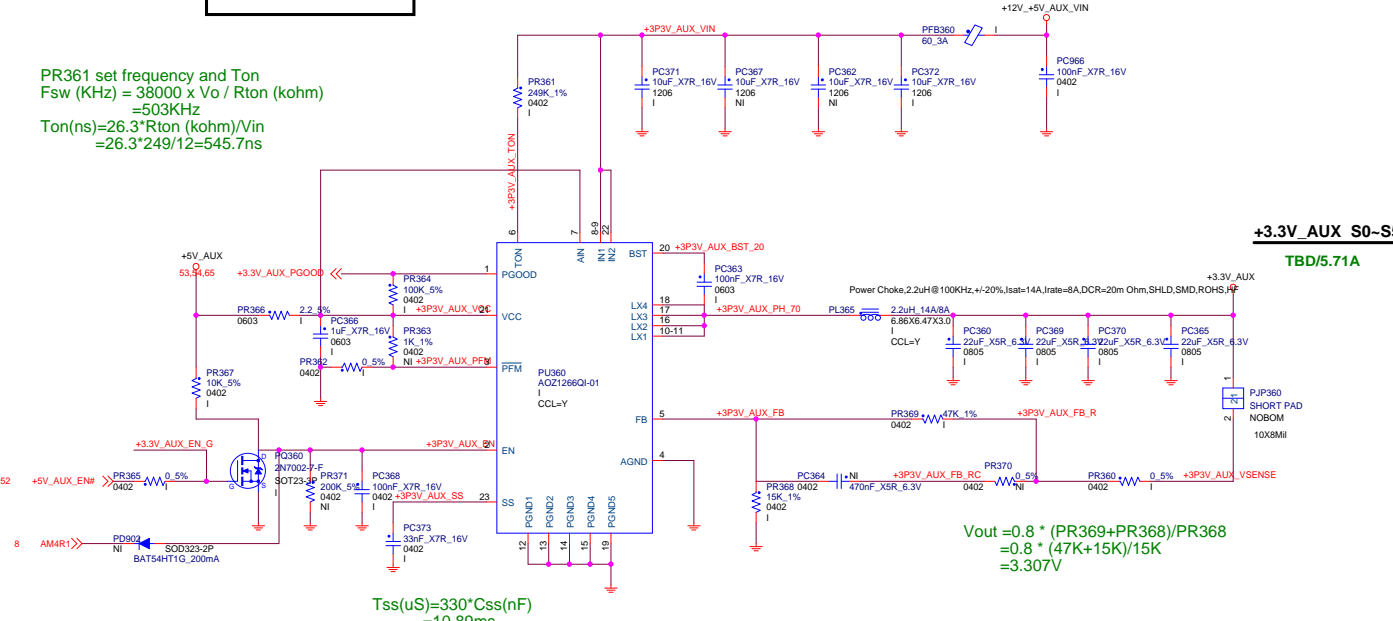
+12V_+5V_AUX_VIN



		HP RESTRICTED (HP RESTRICTED SECRET)	
DRAWN BY		FOXCONN	
Title		+3.3V_LPS	
Size	Document Number	Rev	
B	854433-000	X2	
Date:	Tuesday, June 20, 2017	Sheet	50 of 68

+3.3V_AUX

PR361 set frequency and Ton
 $F_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$
 $= 503 \text{ KHz}$
 $Ton \text{ (ns)} = 26.3 \times R_{ton} \text{ (kohm)} / V_{in}$
 $= 26.3 \times 249 / 12 = 545.7 \text{ ns}$


$$\begin{aligned} V_{out} &= 0.8 * (PR369 + PR368) / PR368 \\ &= 0.8 * (47K + 15K) / 15K \\ &= 3.307V \end{aligned}$$

+3.3V_AUX S0~S5

TBD/5.71A

www.aitech1.ru

+5V_AUX & +5V_DUAL

S3,S0 : H
S4,S5 : L

40,43 5V_DUAL_EN >>

+5V_AUX_EN# >>

Deep SLP,S5,S4,S3 : L
S0: H

9,38,40,43,45,48 SLP_S3# >>


43,46 PWROK_PS >>

+5V_DUAL S0~S3

TBD/1A

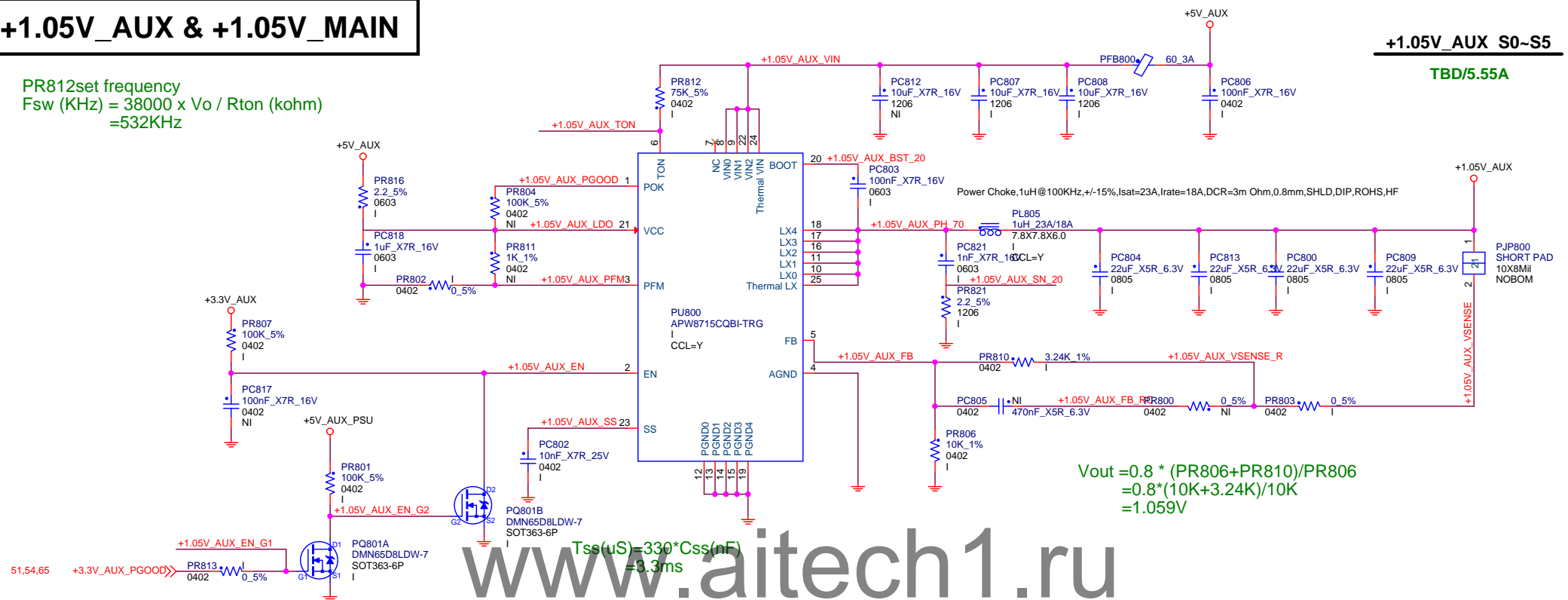
+5V_AUX S0~S5

TBD/11A

 HEWLETT PACKARD		HP RESTRICTED (HP RESTRICTED SECRET) THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP).DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
		DRAWN BY FOXCONN	
Title +5V_DUAL			
Size B	Document Number 828985-000		Rev X2
Date: Tuesday, June 20, 2017		Sheet 52 of 68	

+1.05V_AUX & +1.05V_MAIN

PR812set frequency
 $F_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$
 $= 532\text{KHz}$



www.aitech1.ru

HP RESTRICTED (HP RESTRICTED SECRET)
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY **Foxconn CMSG DWHD**

Title **+1.05V_AUX / +1.05V_MAIN**

Size B Document Number 854433-000 Rev **X2**

Date: Tuesday, June 20, 2017 Sheet 53 of 68

1.8V_AUX & 1.8V_MAIN

PR516 set frequency and Ton
 $F_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$
 $= 527 \text{ KHz}$
 $Ton(ns) = 26.3 \times R_{ton} \text{ (kohm)} / V_{in}$
 $= 26.3 \times 130 / 12 = 284.9ns$

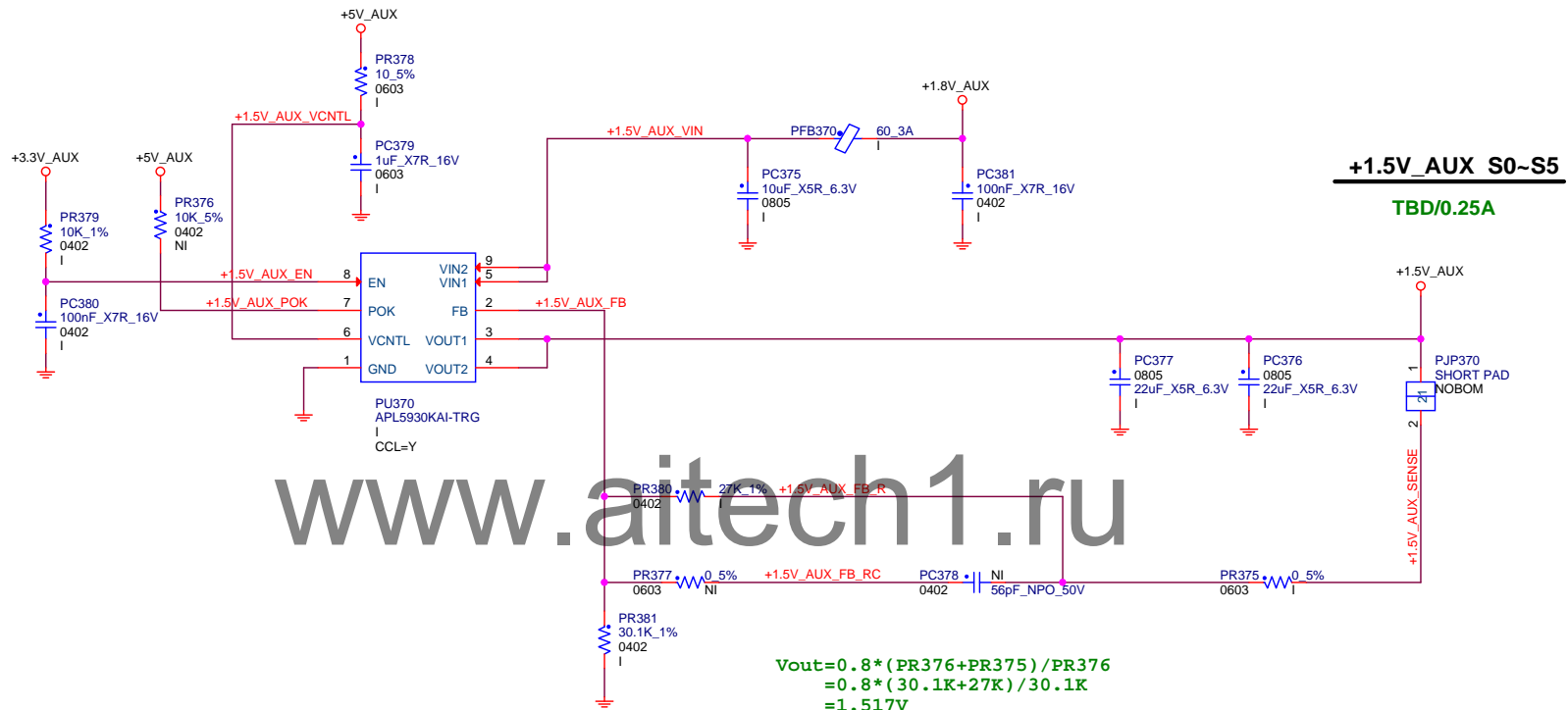
+1.8V_AUX S0-S5
 TBD/2.75A

$V_{out} = 0.8 \times (PR503 + PR506) / PR506$
 $= 0.8 \times (12.7K + 10K) / 10K$
 $= 1.8V$

$T_{ss}(uS) = 330 \times C_{ss}(nF)$
 $= 3.3ms$

+1.8V_MAIN
 2A/TBD

+1.5V_AUX



$$V_{out} = 0.8 * (PR376 + PR375) / PR376$$

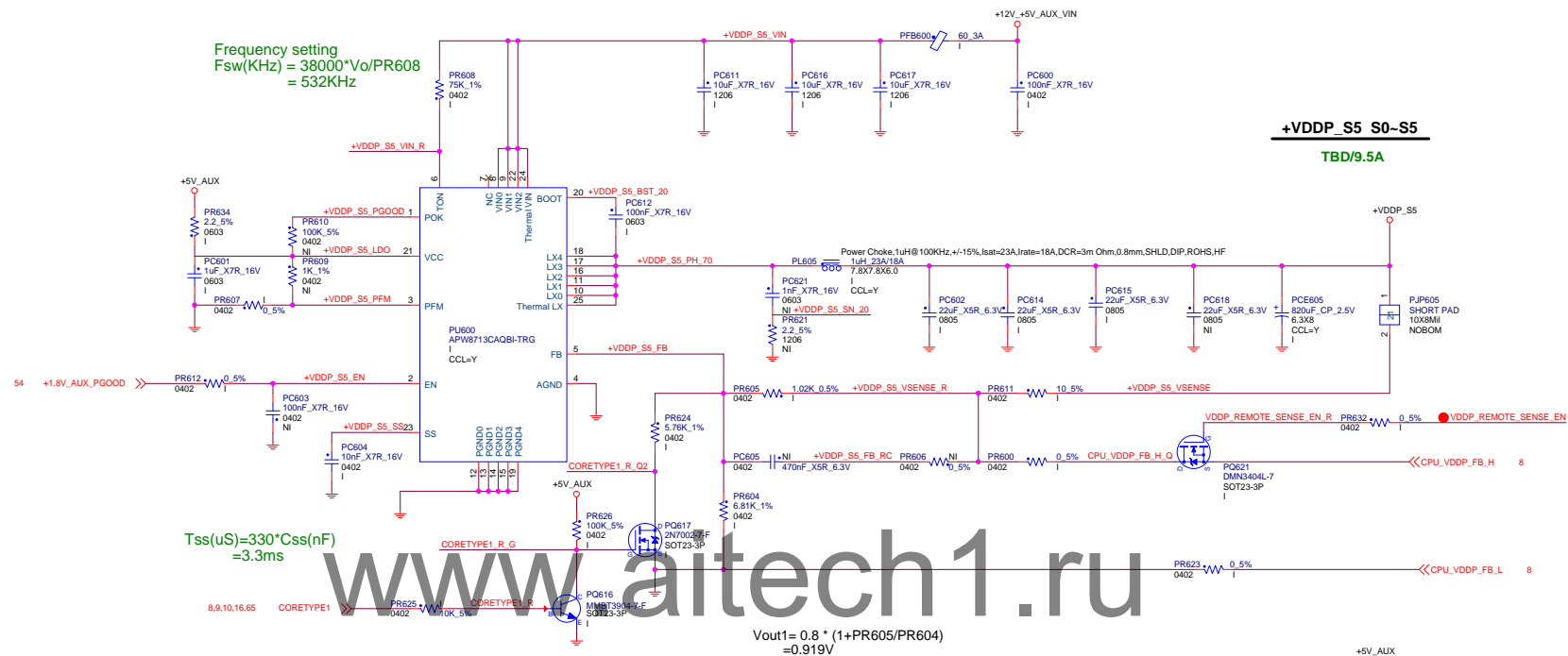
$$= 0.8 * (30.1K + 27K) / 30.1K$$

$$= 1.517V$$

PU410 IC Pd=3w
RqJA=40°C/W
actual
Pd=(1.8-1.5)*0.25=0.075w

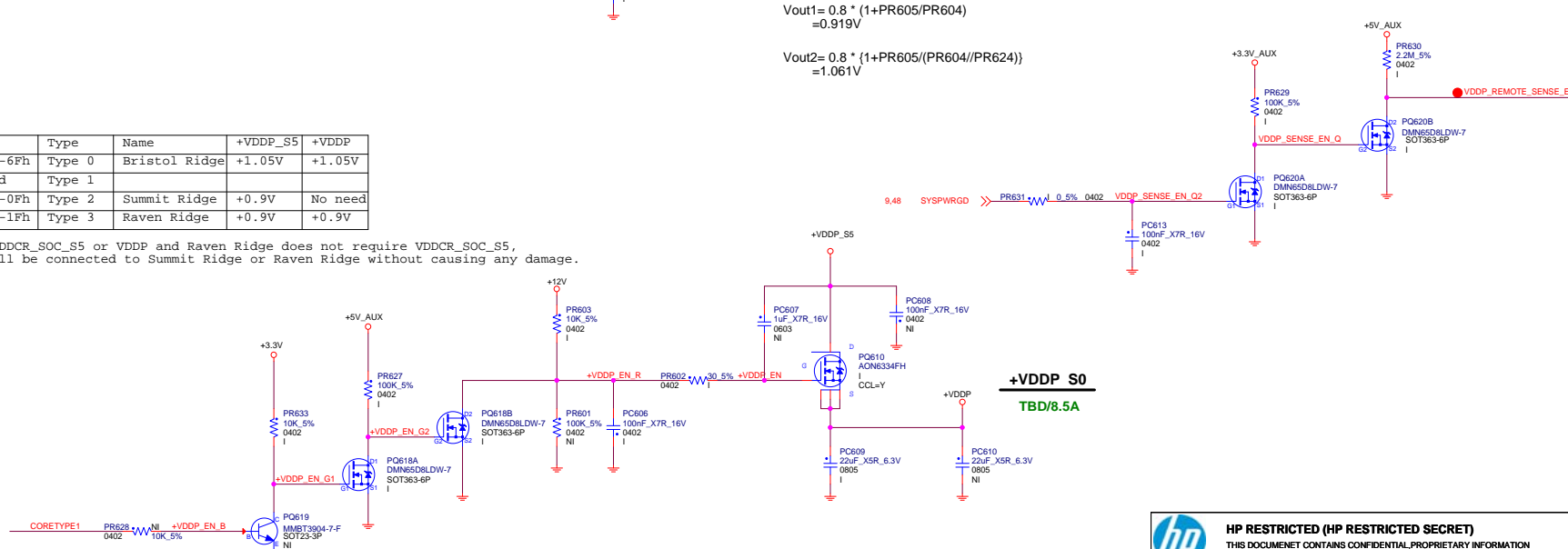
		HP RESTRICTED (HP RESTRICTED SECRET)	
		THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
DRAWN BY		FOXCONN	
Title		+1.5V_AUX	
Size B	Document Number	Rev	
	854433-000	X2	
Date:	Tuesday, June 20, 2017	Sheet	55 of 68

+VDDP_S5 & +VDDP

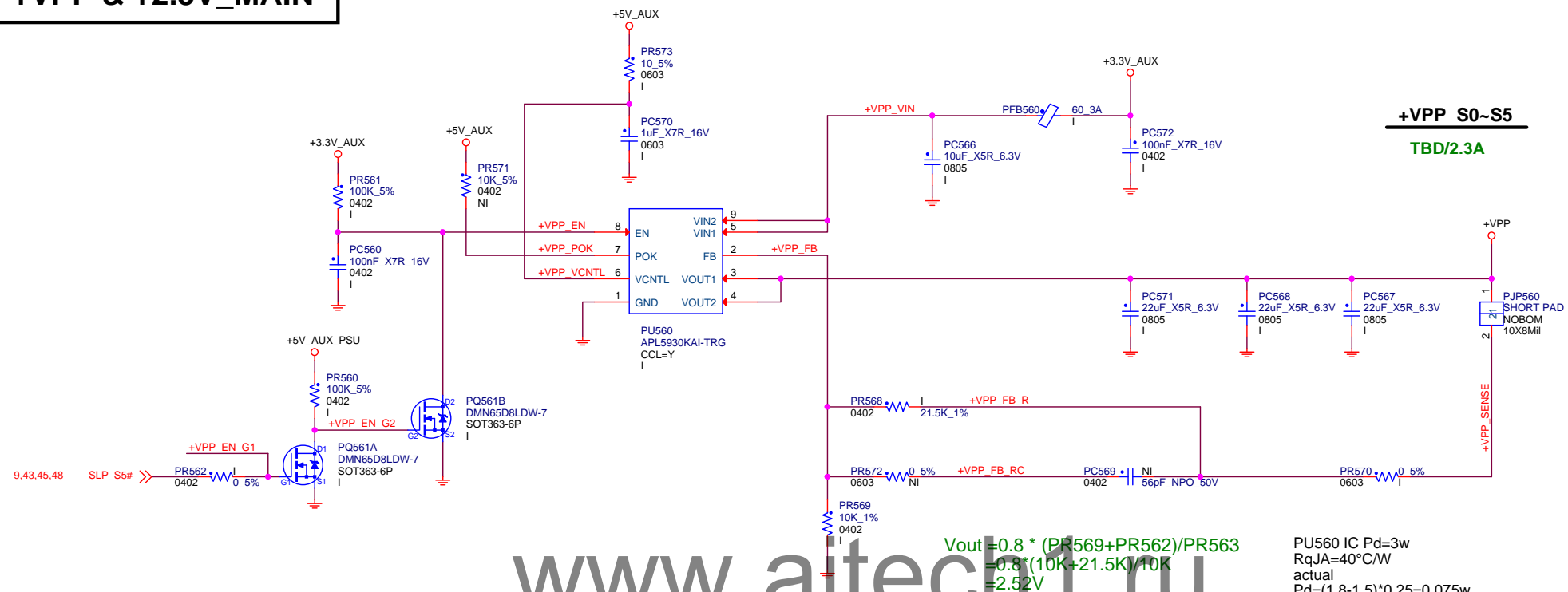


CORETYPE1	CORETYPE0	Family	Type	Name	+VDDP_S5	+VDDP
0	0	15h 60h-6Fh	Type 0	Bristol Ridge	+1.05V	+1.05V
0	1	Reserved	Type 1			
1	0	17h 00h-0Fh	Type 2	Summit Ridge	+0.9V	No need
1	1	17h 10h-1Fh	Type 3	Raven Ridge	+0.9V	+0.9V

Summit Ridge does not require VDDCR_SOC_S5 or VDDP and Raven Ridge does not require VDDCR_SOC_S5, however, these supplies can still be connected to Summit Ridge or Raven Ridge without causing any damage.

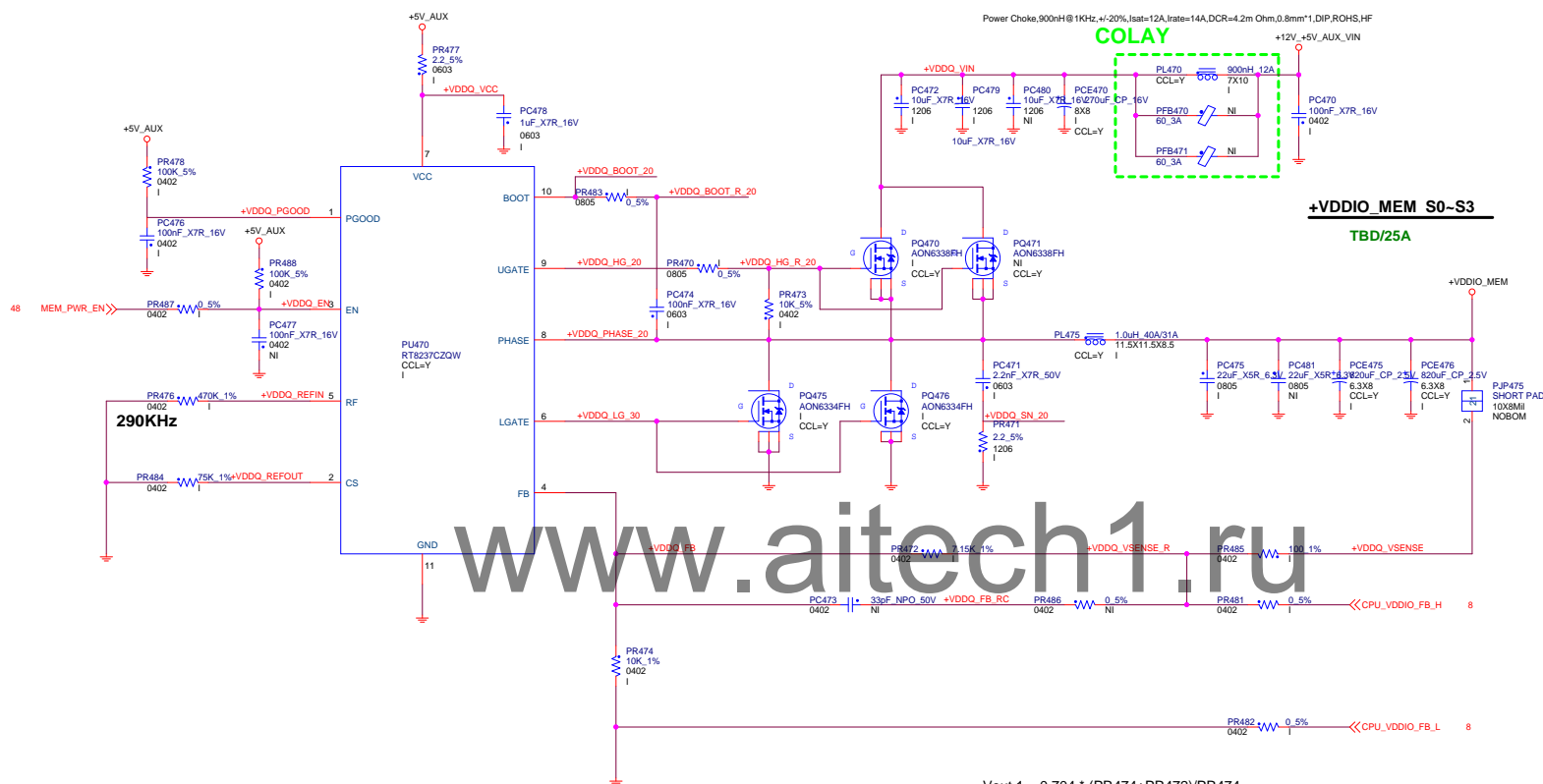


+VPP & +2.5V_MAIN



		HP RESTRICTED (HP RESTRICTED SECRET)	
		THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
DRAWN BY		FOXCONN	
Title		+VPP & +2.5V_MAIN	
Size B	Document Number	Rev	
	854433-000	X2	
Date:	Tuesday, June 20, 2017	Sheet	57 of 68

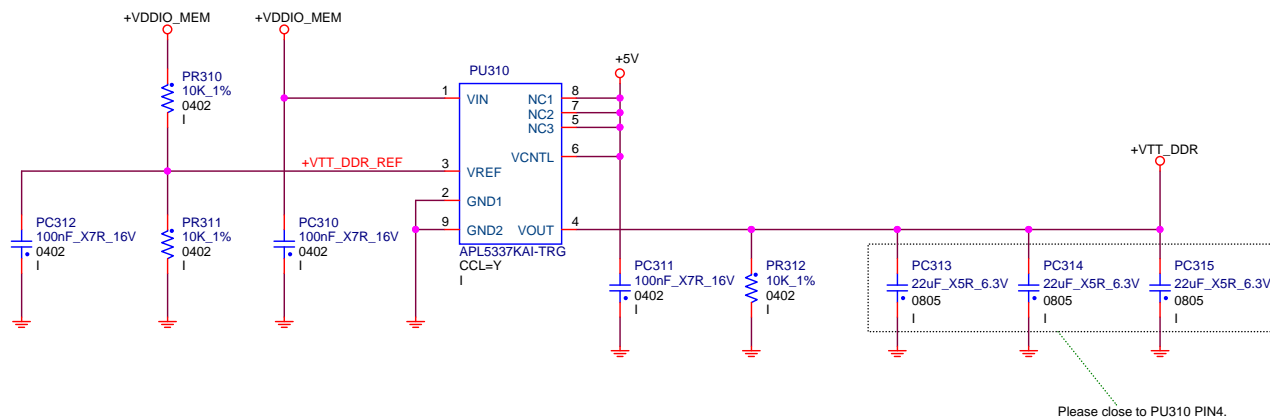
+VDDIO_MEM



$$\begin{aligned} V_{out1} &= 0.704 * (PR474+PR472)/PR474 \\ &= 0.704 * (10K+7.15K)/10K \\ &= 1.207V \end{aligned}$$

$$\begin{aligned} I_{\text{ocp}} &= 10\mu\text{A} \cdot R_{\text{cs}} / (8 \cdot R_{\text{dson}}) + I_{\text{ripple}} / 2 \\ &= 10\mu\text{A} \cdot 150\text{K} / (8 \cdot 5\text{mohm}) + (12 - 1.2) \cdot 1.2 / 2 \cdot 1\mu\text{h} \cdot 290\text{kHz} \cdot 12 \\ &= 39.36\text{A} \end{aligned}$$


+VTT_DDR



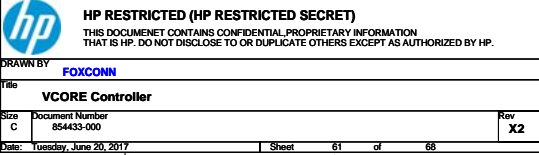
+VTT_DDR S0~S3

0.75A/1A

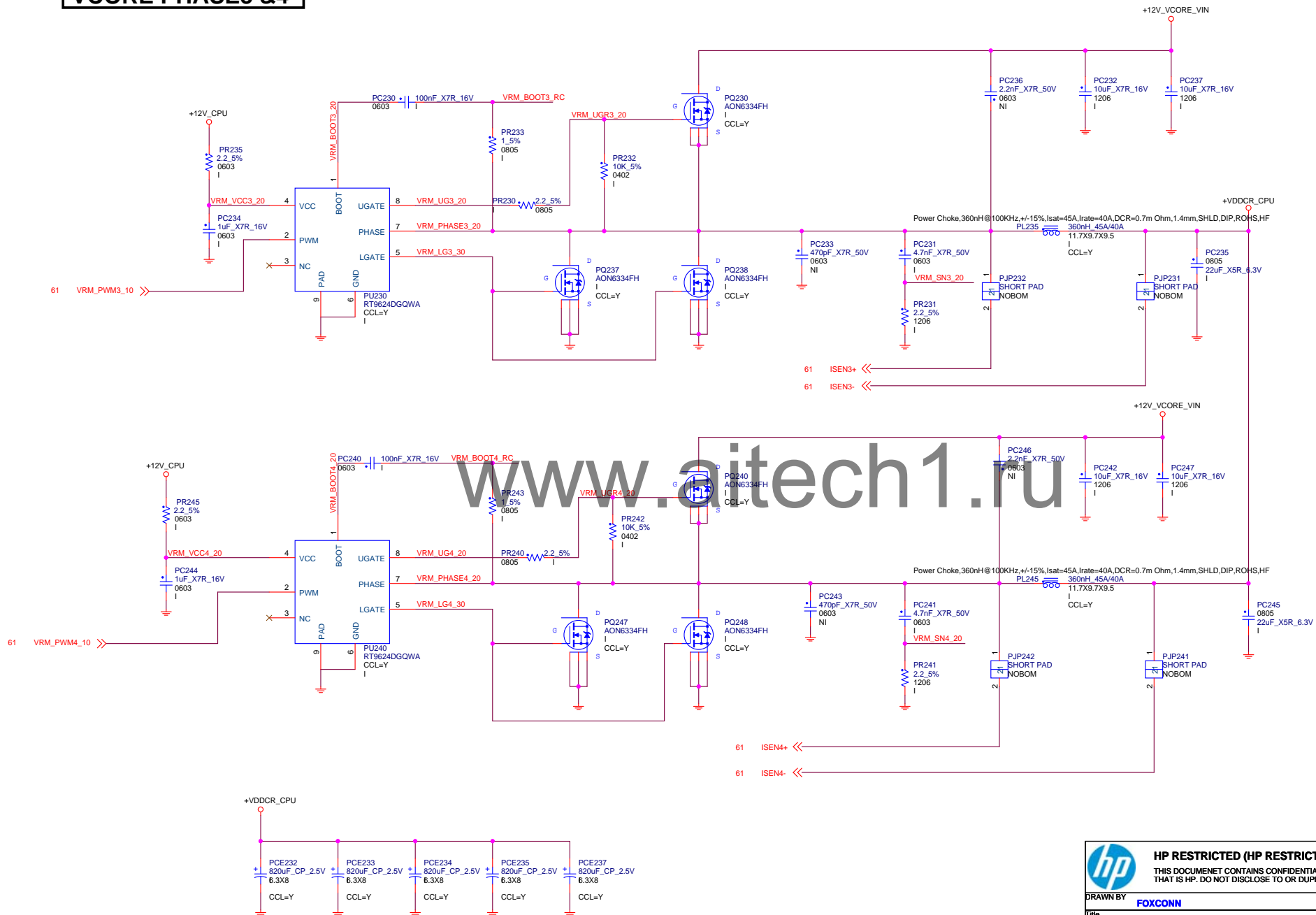
www.aitech1.ru

		HP RESTRICTED (HP RESTRICTED SECRET)	
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.			
DRAWN BY		FOXCONN	
Title		+VTT_DDR	
Size B	Document Number	Rev	
	854433-000	X2	
Date:	Tuesday, June 20, 2017	Sheet	59 of 68

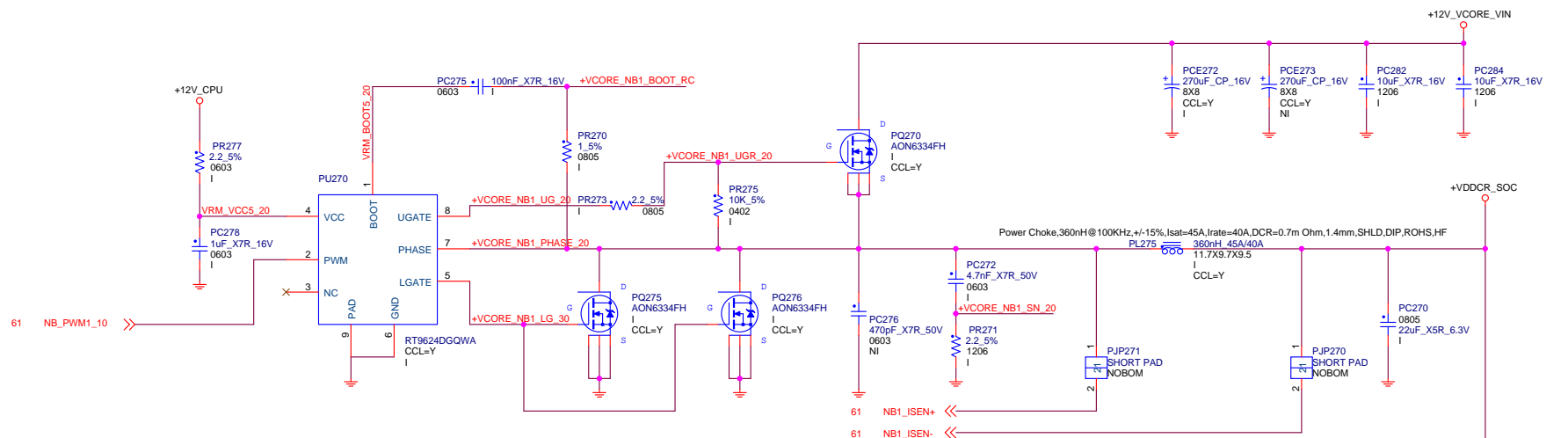
www.aitech1.ru



VCORE PHASE3 &4

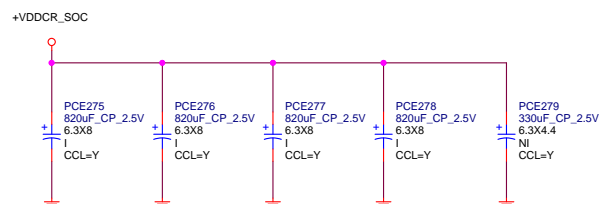
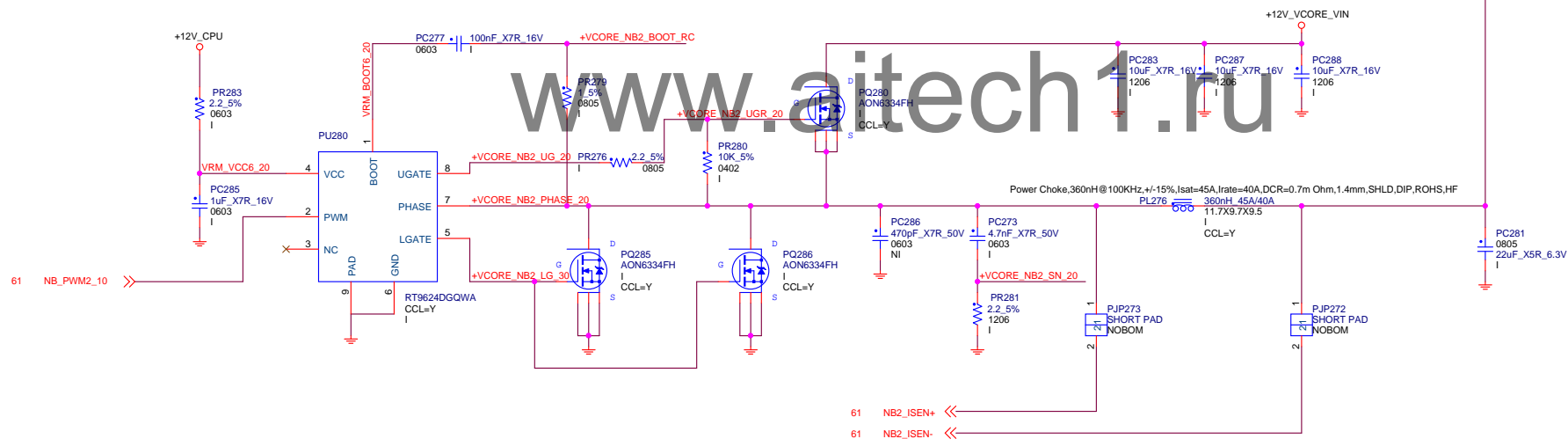


+VDDCR_SOC PHASE1~2



+VDDCR_SOC

Summit Ridge:20A/30A 95W
Bristol Ridge:50A/75A 65W



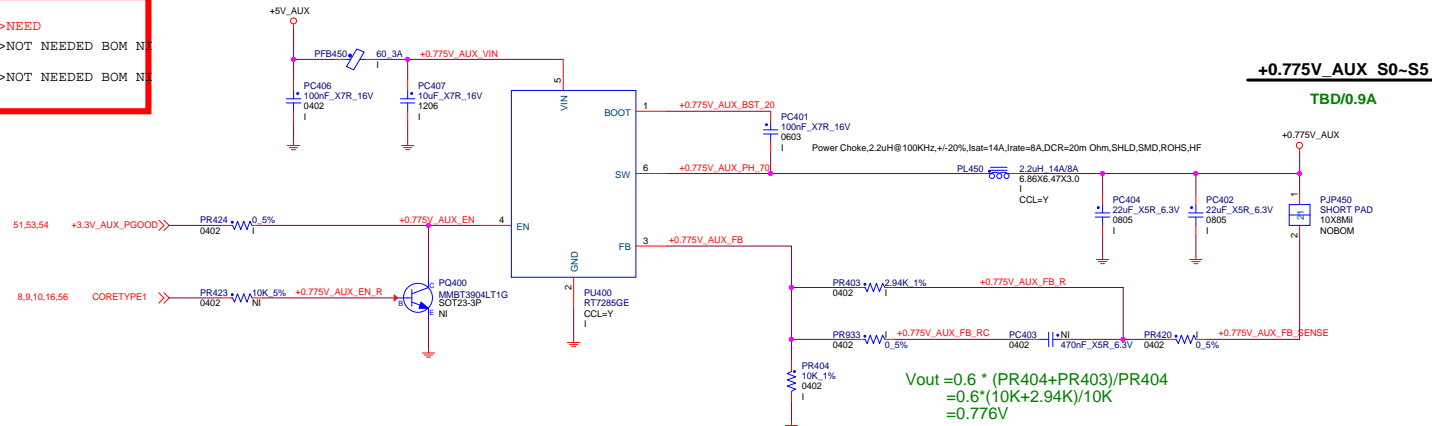
HP Restricted Secret.

		HP RESTRICTED (HP RESTRICTED SECRET)	
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.			
DRAWN BY FOXCONN			
Title VDDNB Driver			
Size	Document Number	Rev	
Custom	854433-000	X2	
Date: Tuesday, June 20, 2017		Sheet	64 of 68

+0.775V_AUX & +VDDCR_SOC_S5

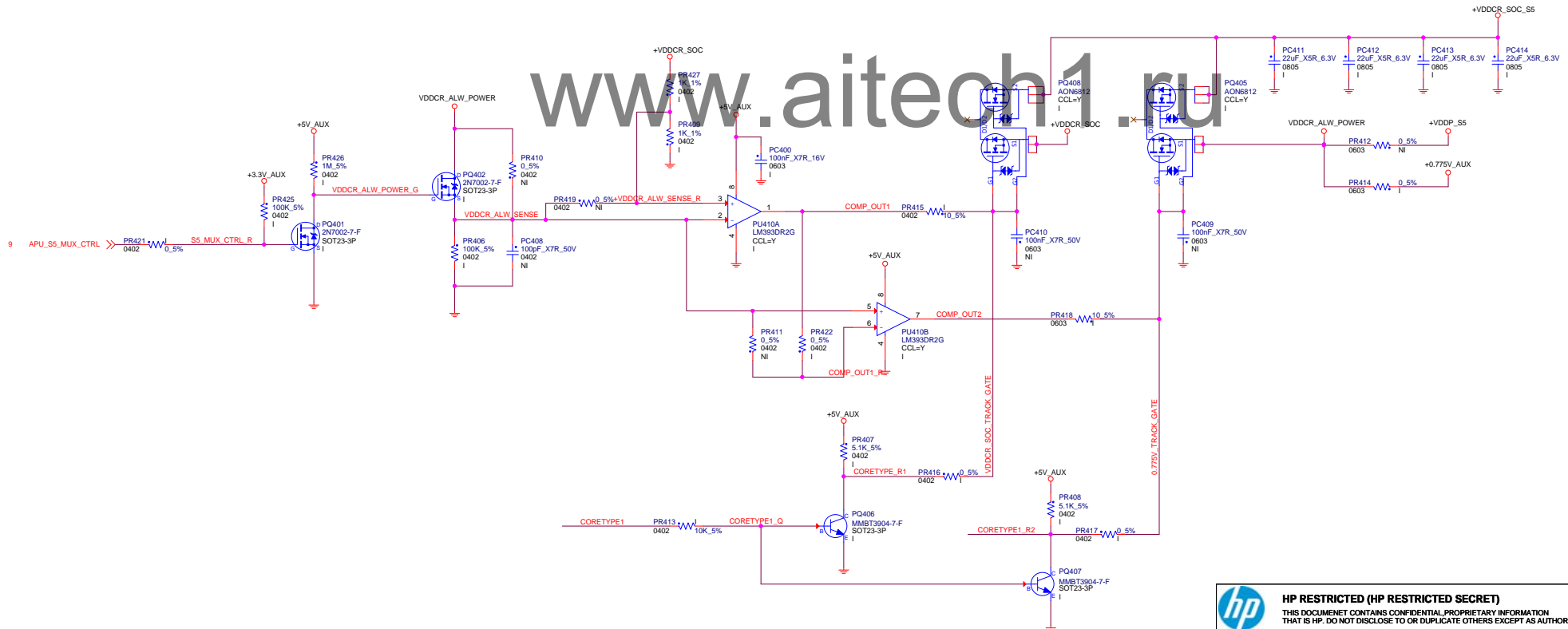
Bristol Ridge /Raven 65W(C) ==>NEED
Summit Ridge 95W(A) ==>NOT NEEDED BOM N
Summit Ridge 65W(B) ==>NOT NEEDED BOM N

S5_MUX_CTRL: S0 -- HIGH
S3/S5 -- LOW
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

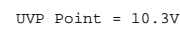


+VDDCR_SOC_S5

TBD/0.2A



www.aitech1.ru



 **HP RESTRICTED (HP RESTRICTED SECRET)**
THIS DOCUMENT CONTAINS CONFIDENTIAL/PROPRIETARY INFORMATION
THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.

DRAWN BY FOXCONN			
Title Current Monitor			
Size	Document Number		Rev
Custom	854433-000		X2
Date:	Tuesday, June 20, 2017	Sheet	66 of 68

[DB to SI](#)

2/25/2017

Page 53: add snubber 1nF+2.2ohm for frequency fail item.

Page 54:add snubber 1nF+2.2ohm for frequency fail item

2/26/2017

Page 61: add AGND, connecting AGND and GND by 0ohm resistor for APU_PWROK noise issue.

Page58:change PC473, PR486 from NI to I for better phase &gain margin.

3/3/2017


Page 52: add +5V_S5 to transfer +5V_AUX for decreasing +5V_AUX_PSU inrush current

[SI to PV](#)

4/29/2017

Page58:change PR476 from 39K to 470K,
PR486 and PC473 from I to NI for Model B&C phase jitter fail item.

www.aitech1.ru

		HP RESTRICTED (HP RESTRICTED SECRET)	
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.			
DRAWN BY FOXCONN			
Title PWR Change list			
Size Custom	Document Number 854433-000		Rev X2
Date: Tuesday, June 20, 2017	Sheet 67	of 68	

0109 Change

SR76 change to 100K for ITE review change
SIO_SMI# change from GP46 to GP47 for GP46 can't map to SMI
Add 48M clock connect to SIO for SIO need
SIO pin128 add 10k pull high to 3.3V for ITE review change

0206 Change

Change U30,U33 AP2161WG-7 to AP2171WG-7, high active
Change U31,U32 AP2822HKETR-G1 to G524B1T11U,high active
Change R1594 to I,R1593 to NI for install UMA driver blackscreen issue
Change XU1_BP to PW35311-002
Change R387 to I(DB installed by PCA note)
Change R435 to 4.7K,R440 1K I, R387 100K I,add R426 100K I(DB implemented by PCA note)
Change R471 pull high from +3.3V_AUX to +3.3V

0209 Change

Add SU1 48MHz clock gen, reserve for SIO CLKIN
Change C573 to NI,R265 to 33ohm,SR43 to 33ohm,add C477 12pf
at PCH side for APU_PCIE_RST# non-monotonic at SIO and PM2 side issue

0220 Change

Add Q2,Q7 HDMI power circuit for HDMI voltage fail issue
Change R207,R408 pull high to +3.3V
Change C177,C265 from NI to I for memory reset signal integrity issue

0224 Change

Add R901 100K ,PC3 luf change to I for T3 sequence issue

0225 Change

Change U31,U32 to R(ds)on= 50m ohm part AP22802AW5-7 for usb power drop issue

0226 Change

Change BBR GPIO from AGPIO5 to EGPIO70, AGPIO5 add R64 pull low for bristol leakage from AGPIO5 issue
Change R266 to I,R269 to NI for board version to SI

0302 Change

Change Audio de-pop circuit ,NI AR66/AR42 add AR70/AR71/AR72/AQ9 ,Add SIO GPIO control

0304 Change

Change AR56 from 22k to 2.2k ohm according vendor suggestion.
Add R900 for M2.2280 pull down

0306 Change

Change Add SR252/SQ11 for USB power control

0308 Change

Add Choke PL806 (DC side) for +5V/ choke L63 for +12V
SWAP TYPE CC pin ESD net for layout
Add SR254/SC24 on SYS Fan PWM net to fix Sys_Fan tach issue
Add SR255/SR256 on SIO SMBUS according ITE suggestion
Change SR89 from NI to I according ITE suggestion

0310 Change

Add Choke L64 for +3.3V noise issue
Add SR257/SC25 on CPU Fan PWM net
Add R999/C2036 on U36 output

0313 Change

Change D4/D6 source same as AD2 for BOM
Change Q60/Q7 source same as SQ7 for BOM

0314 Change

Change LU4/LU5 from I to NI according EMC test result

0315 Change

Change R362 from I to NI according BIOS requirement

0317 Change

Change U28 from I to NI

SI to PV change

0330 Change

Add R457 10k pull high for USB3_OC_REAR#
Location L6,L8,L14,L16,L18,L24 change to NI, Location R63,R218,R231,R232,R286,
R287,R296,R297,R303,R306,R325,R327 change to I

0412 Change

page16,HDT circuit bom change to I for PV will remove proto part
Change R266,R260 to NI,R269,R258 to I for PV reversion ID

CN1 main source change to FOXCONN_HSC1040-K0000-7H ,no cover part
BM1,BM2 main source can't purchase, change to SPEEDGOLD_SG428
HDMI1,HDMI2 main source change to tape and reel package,ASTRON_369FA19-3N026D-H
Change U36 related 48M circuit to NI, change SR67 to I
for 48M clock source change to external osc

0427 Change

Change AC13,AC15,AC20,AC21 to 22uf MLCC For fix rear
MIC and line in re-tasking THD+N margin pass
Change PD IC from CYPD4125 to CP8691ATT for CP8691ATT is FW6.4 PN
change PQ452 to low Rdson part AOS_AON6334FH For USB 5V drop optimize
Add Q56,R478,R479 at HDMI power For HDMI have risk to shutdown when hot plug
Change SR254,SR257 to 0ohm for PWM Vlow is 0.4V
Change SR65 to NI for COPEN# should be high

0509 Change

change AU1,U29,U34,U11 FXN PN from -G to -H
change BZ1 to HUA-JIE_PAC-WT-1205-HF HF part

PV to SMVB change

0526 Change

Change R266 to I,R269 to NI for board version change to SMVB
page16,HDT circuit bom change to PROTO for SMVB no need debug port

0610 Change


change C476 100pf to I for PM_PCIRST# NMV

0613 Change

Change PC613 to I for syspwrgd signal NMV
Add PCB material IT-158TC,ML1 in description

0620 Change

Change LR13 to I for LAN loss issue

		HP RESTRICTED (HP RESTRICTED SECRET)	
THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS HP. DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.			
DRAWN BY FOXCONN			
Title Schematic Change List			
Size C	Document Number 921622-000	Rev X2	
Date: Wednesday, June 21, 2017		Sheet 1	of 68